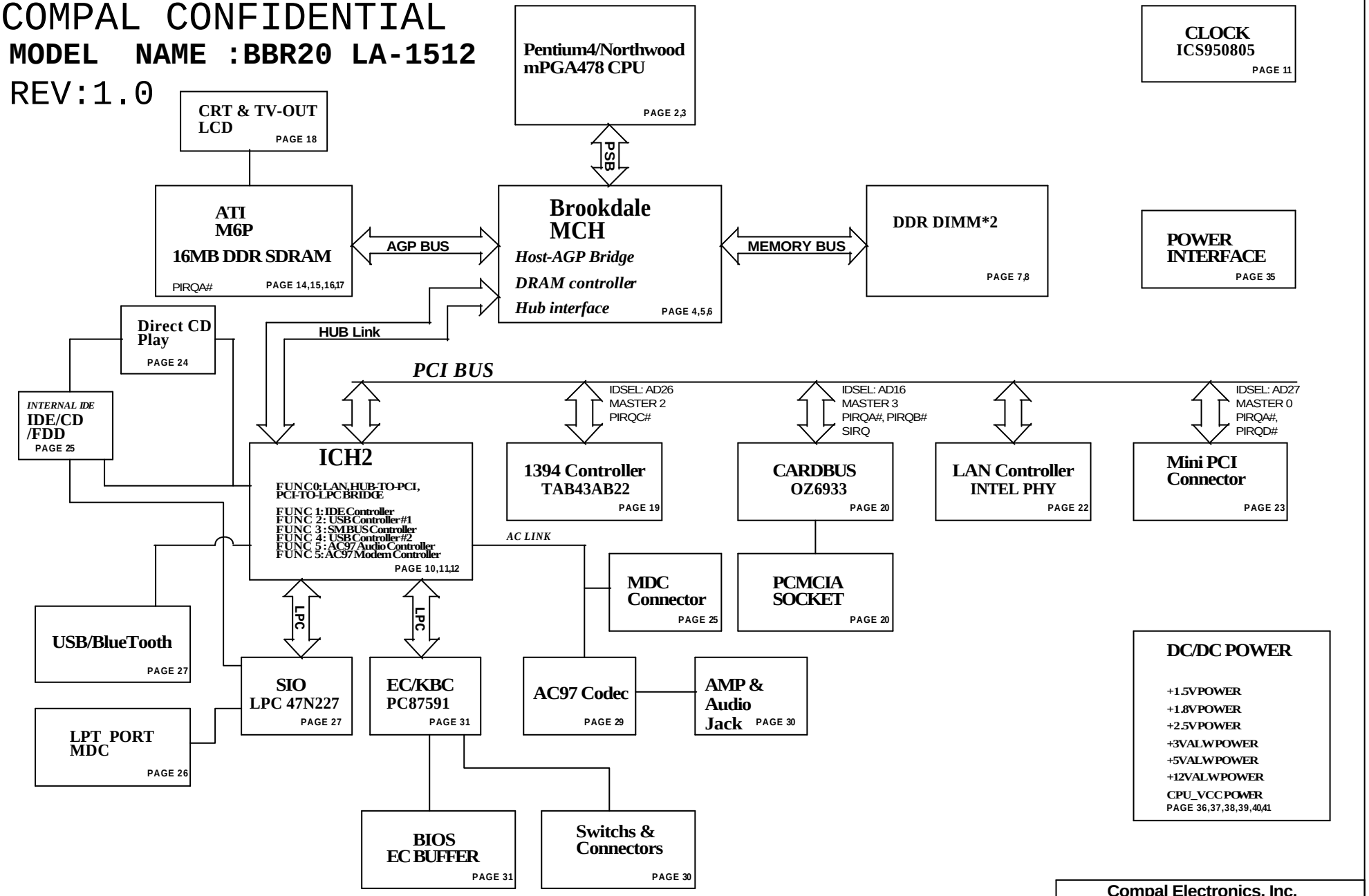
COMPAL CONFIDENTIAL

MODEL NAME :BBR20 LA-1512

REV:1.0



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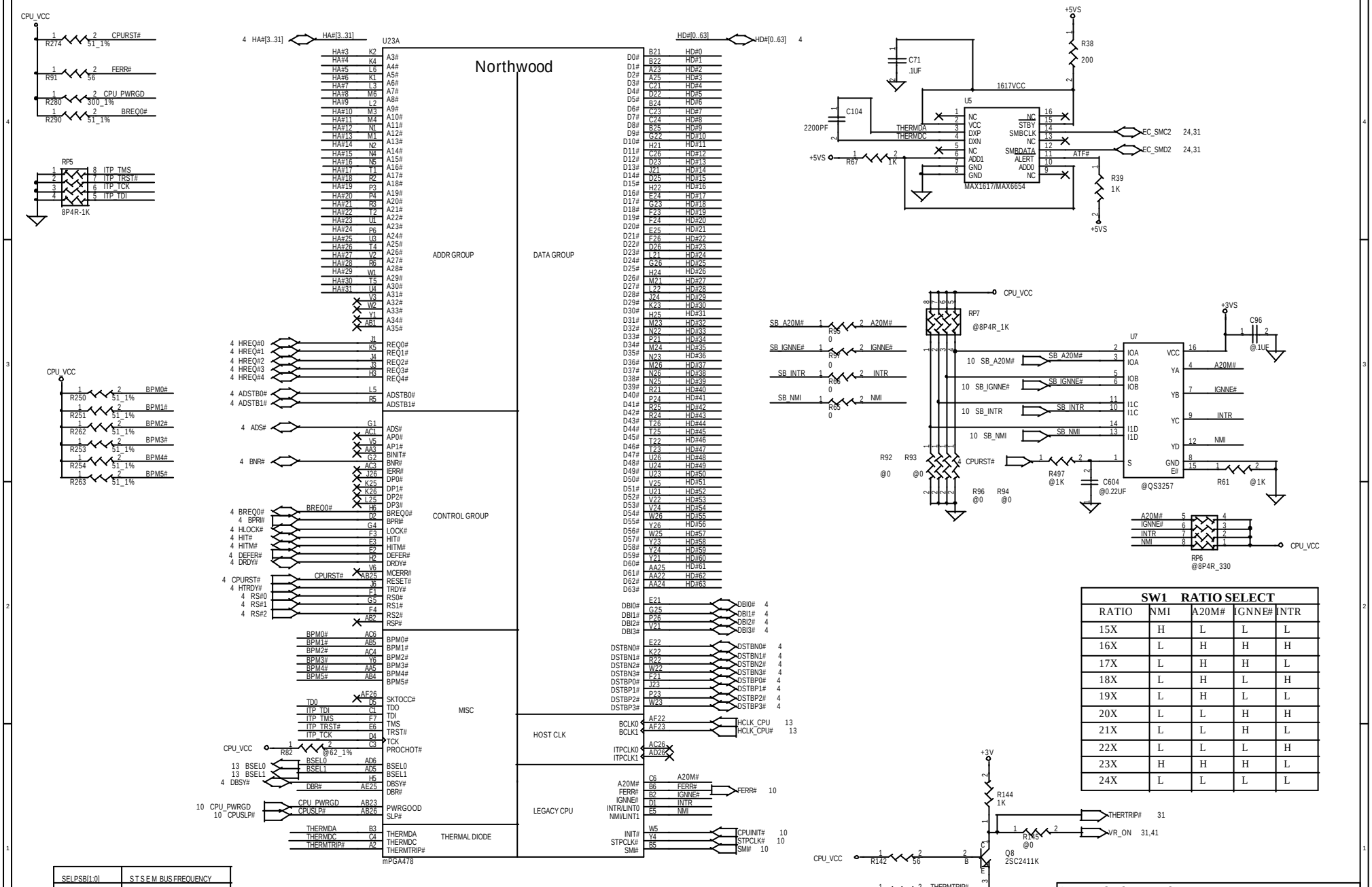

SW1 RATIO SELECT				
RATIO	NMI	A20M#	IGNNE#	INTR
15X	H	L	L	L
16X	L	H	H	H
17X	L	H	H	L
18X	L	H	L	H
19X	L	H	L	L
20X	L	L	H	H
21X	L	L	H	L
22X	L	L	L	H
23X	H	H	H	L
24X	L	L	L	L

SELPSB[1:0]	STSEM BUS FREQUENCY
00	100MHZ
01	RESERVED
10	RESERVED
11	RESERVED

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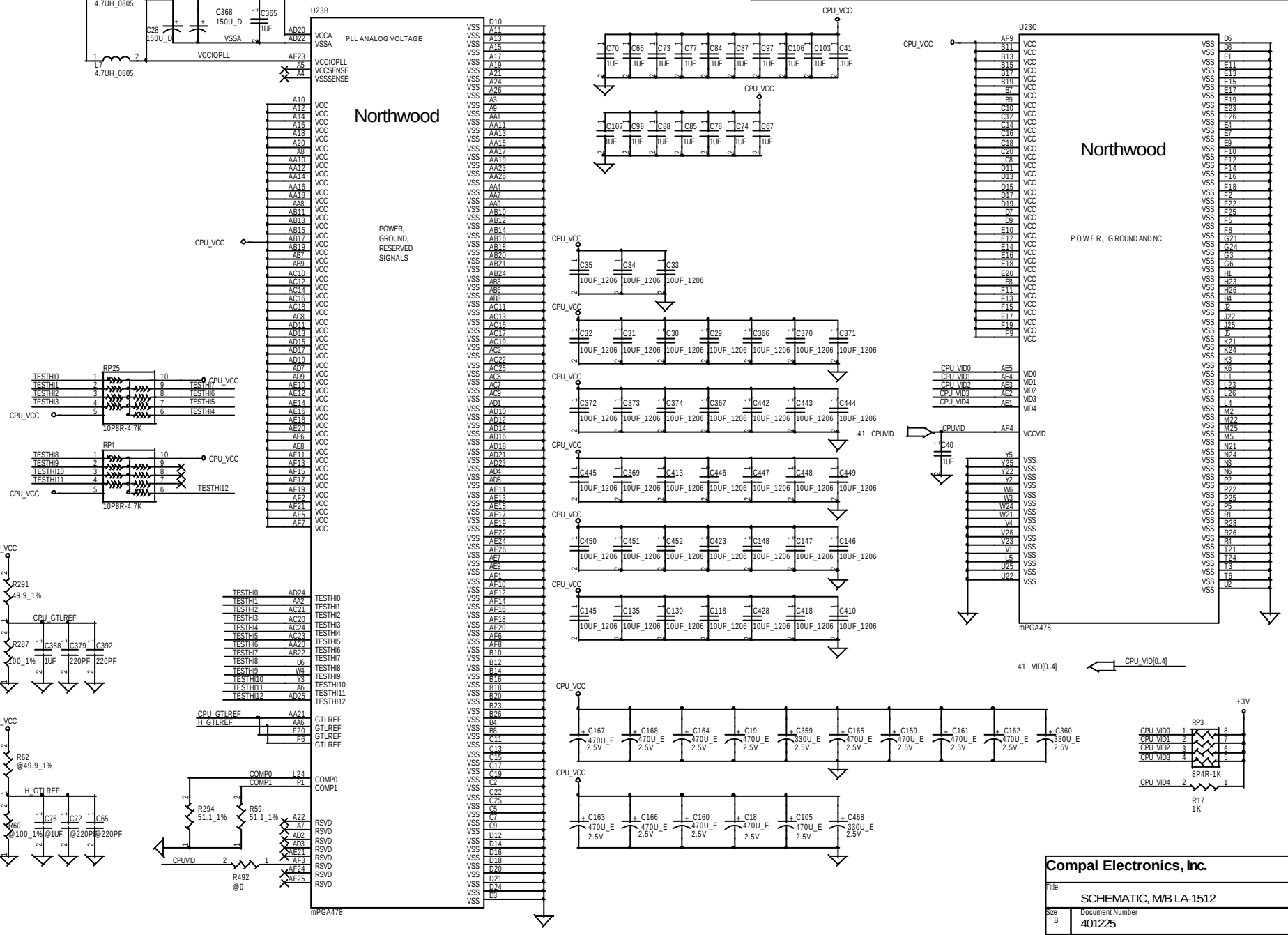

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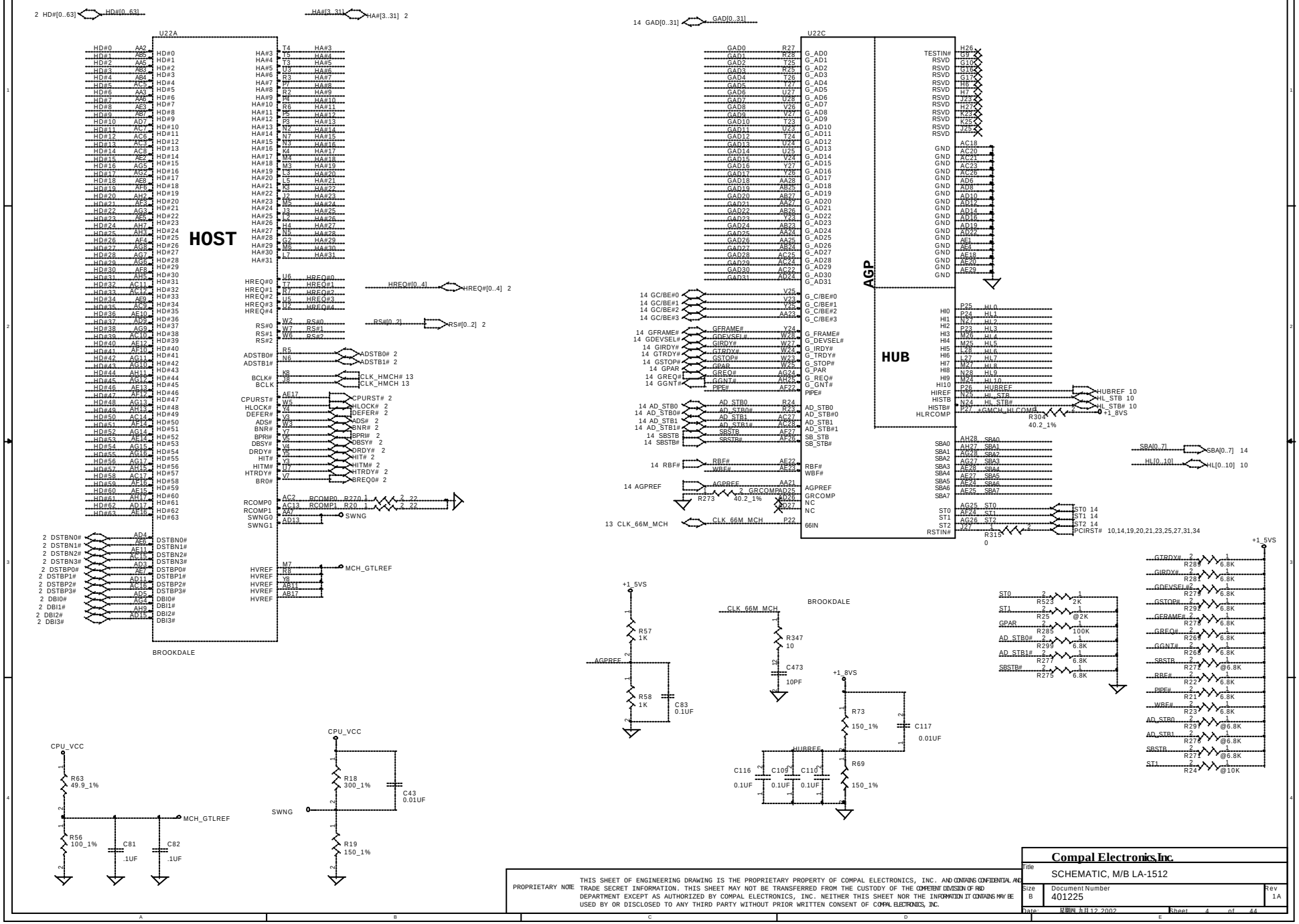
MC-1/3(GTL+,AGP,HUB)



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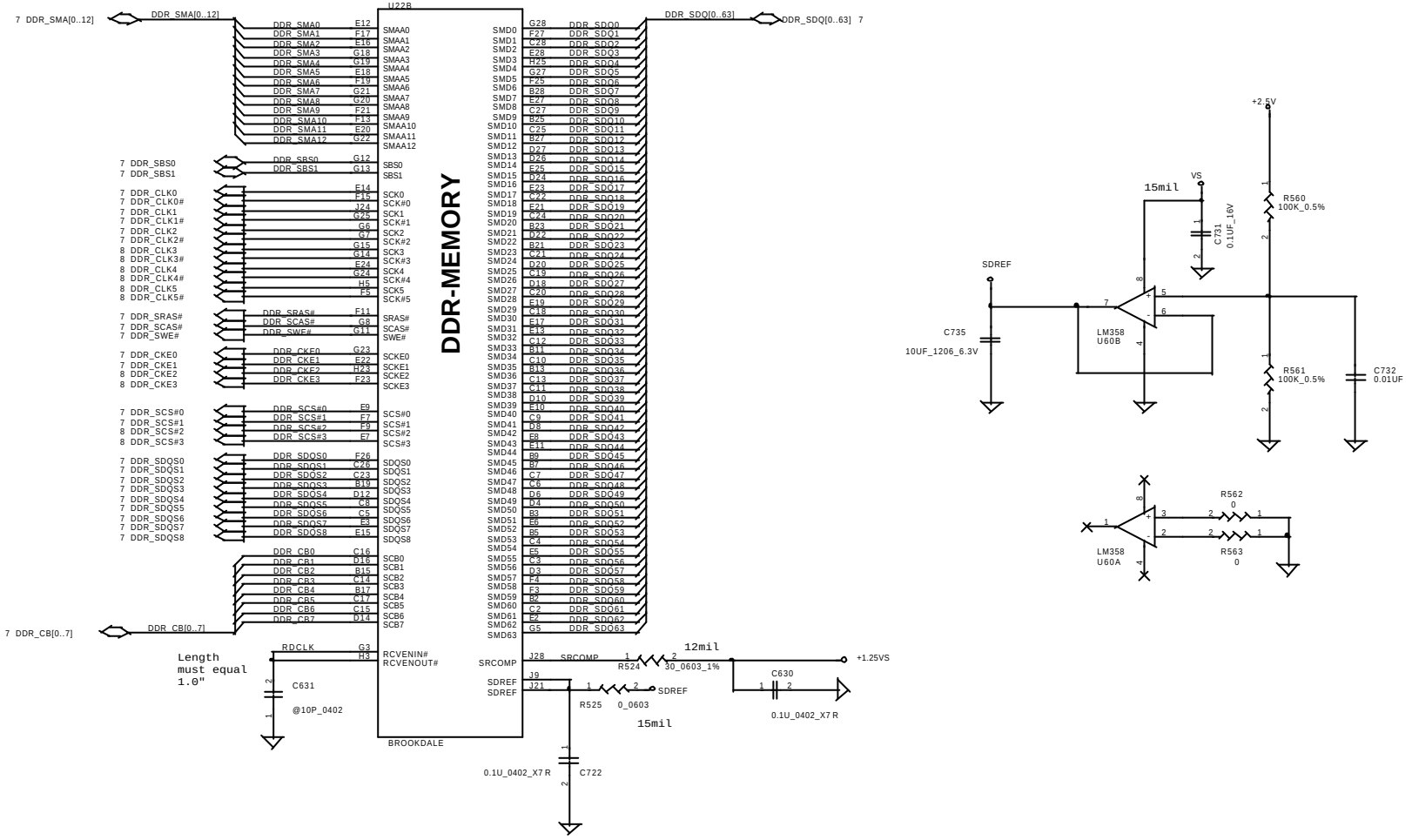
MCH-2/3(SDRAM)



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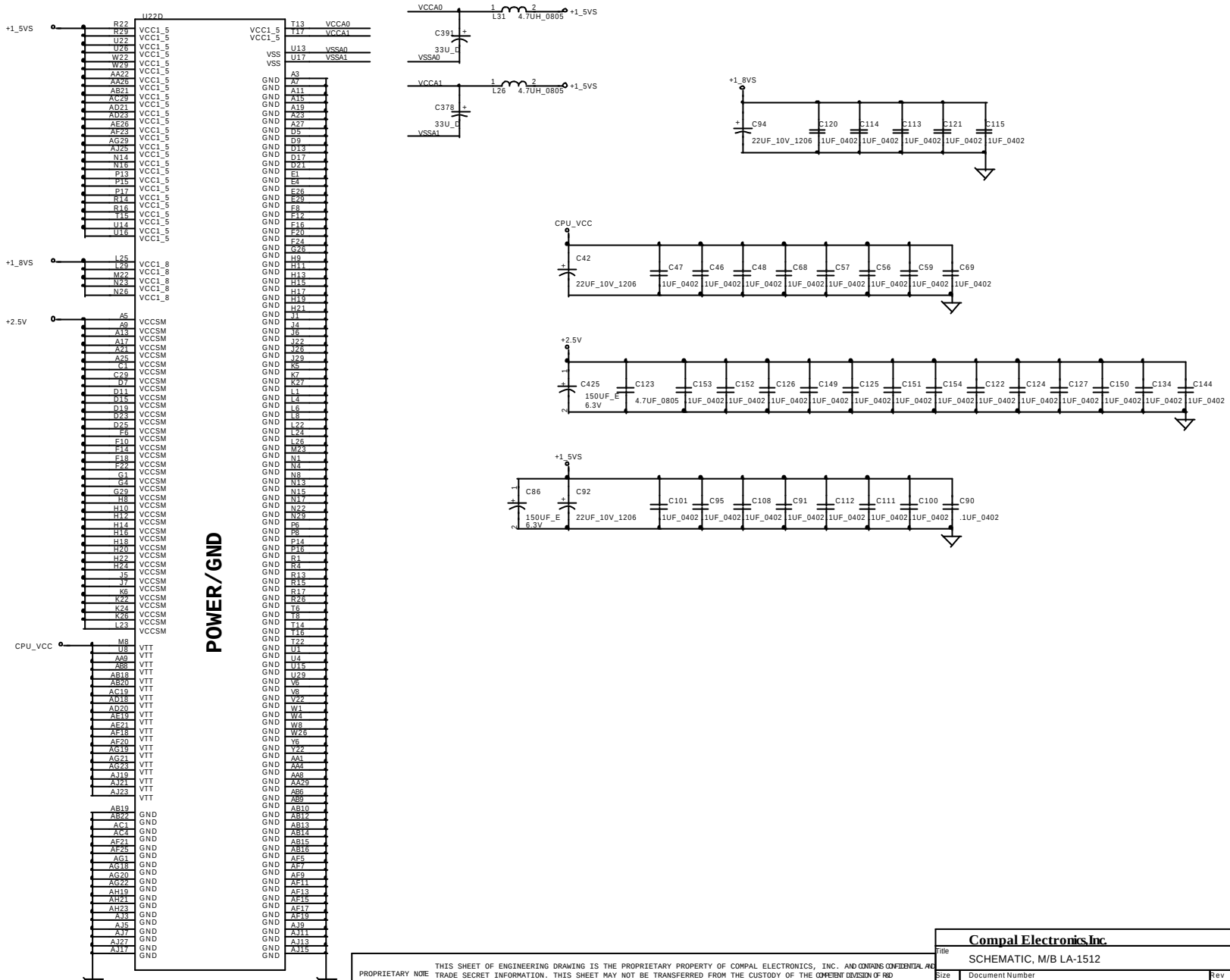
MCH-3/3(Power)



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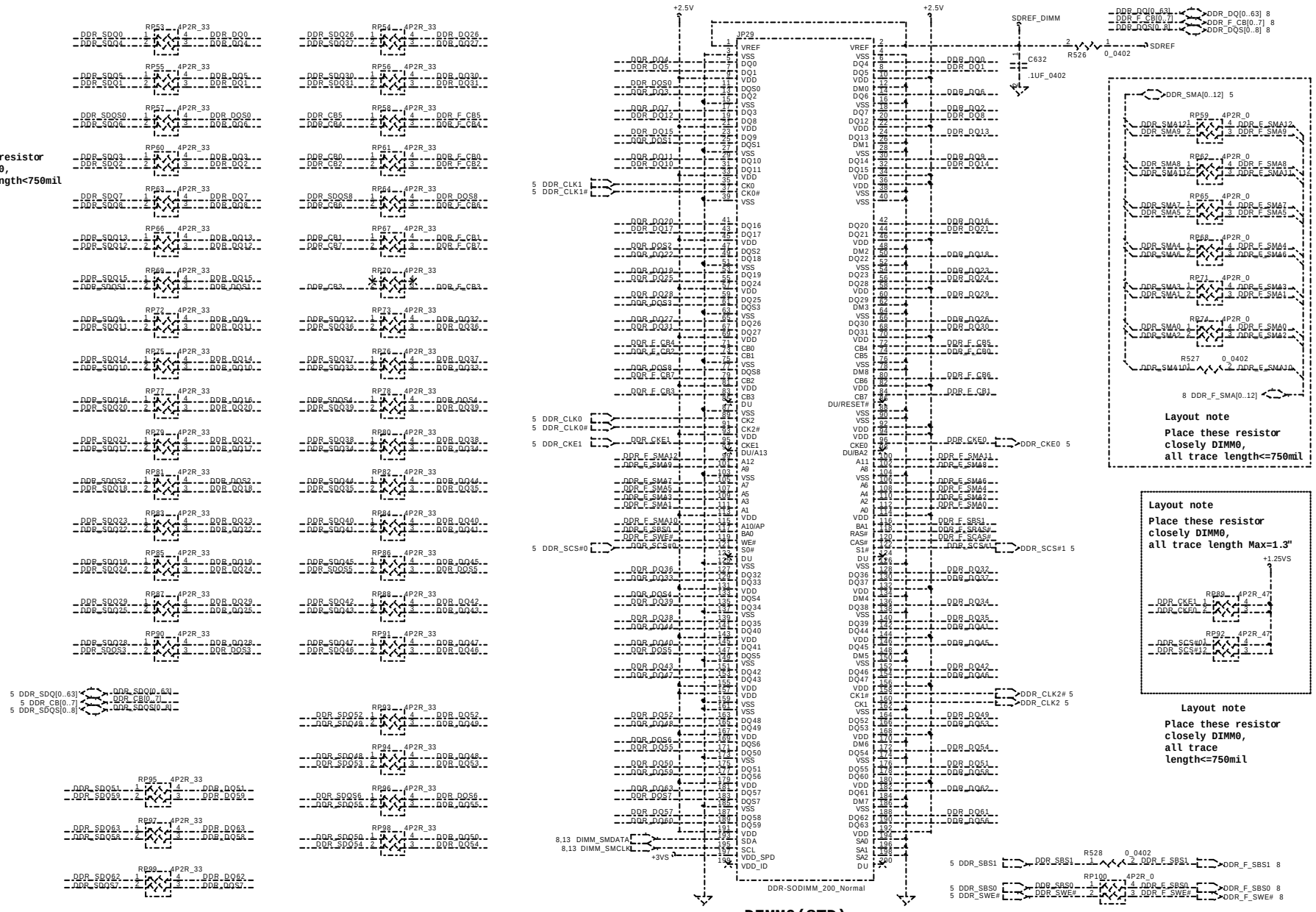

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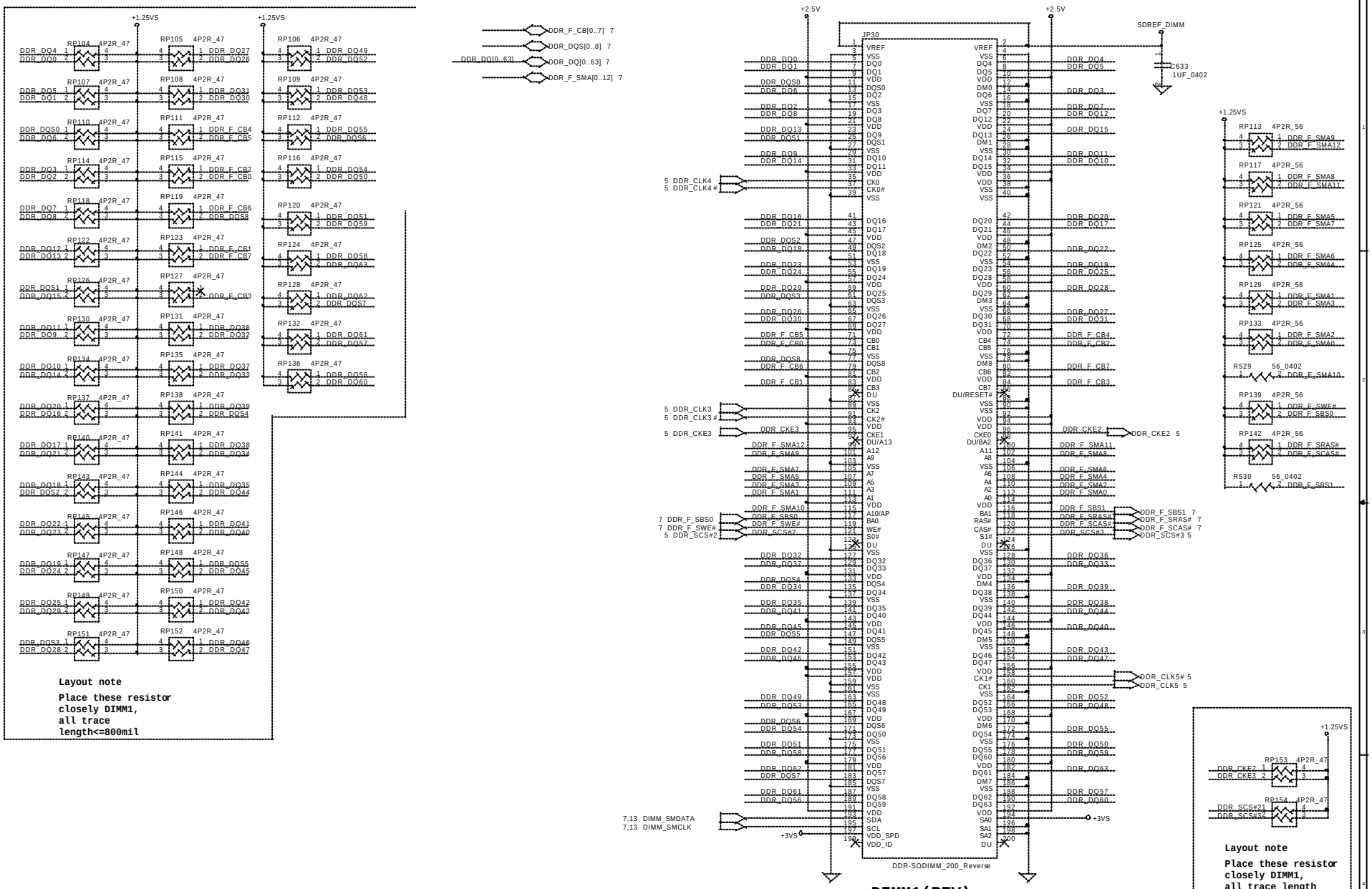

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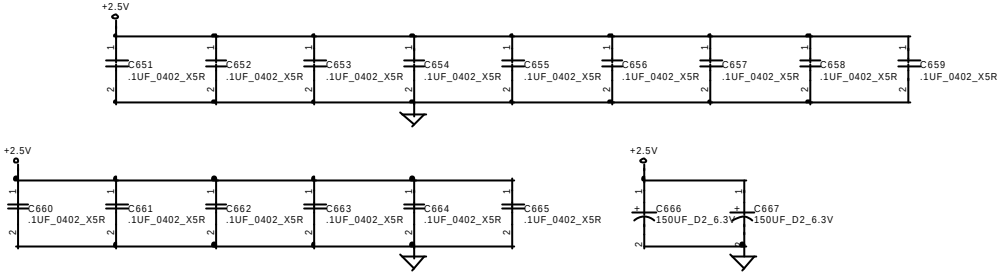
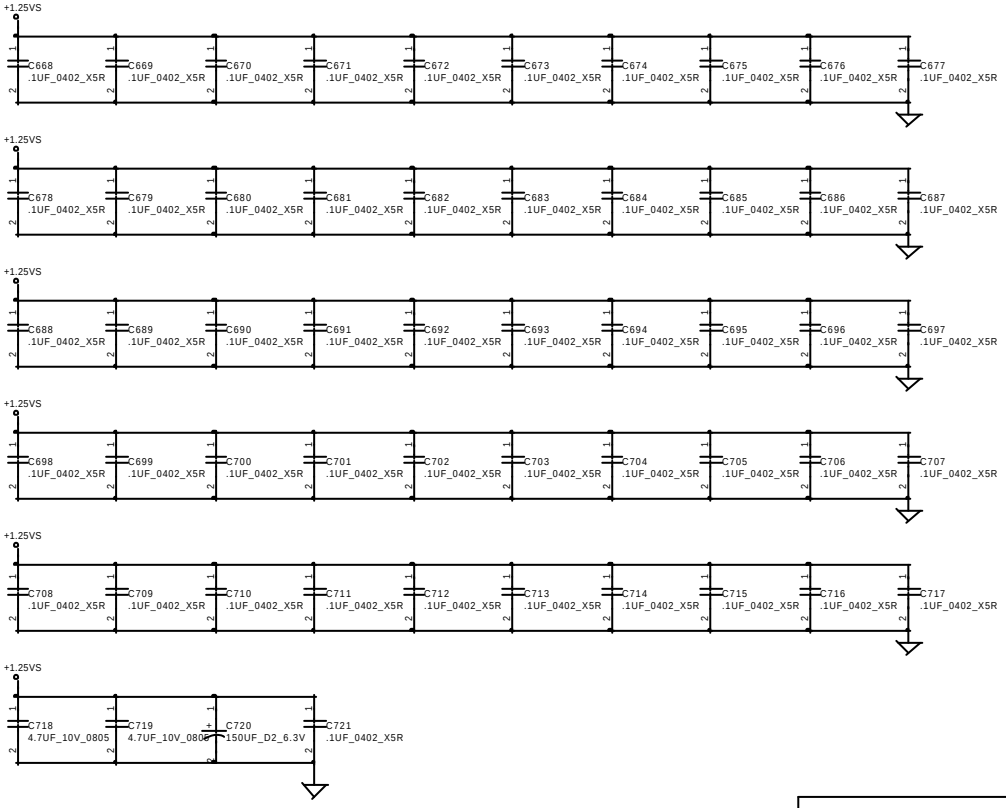
Layout note :
Distribute as close as possible to DDR-SODIMM.



Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25V



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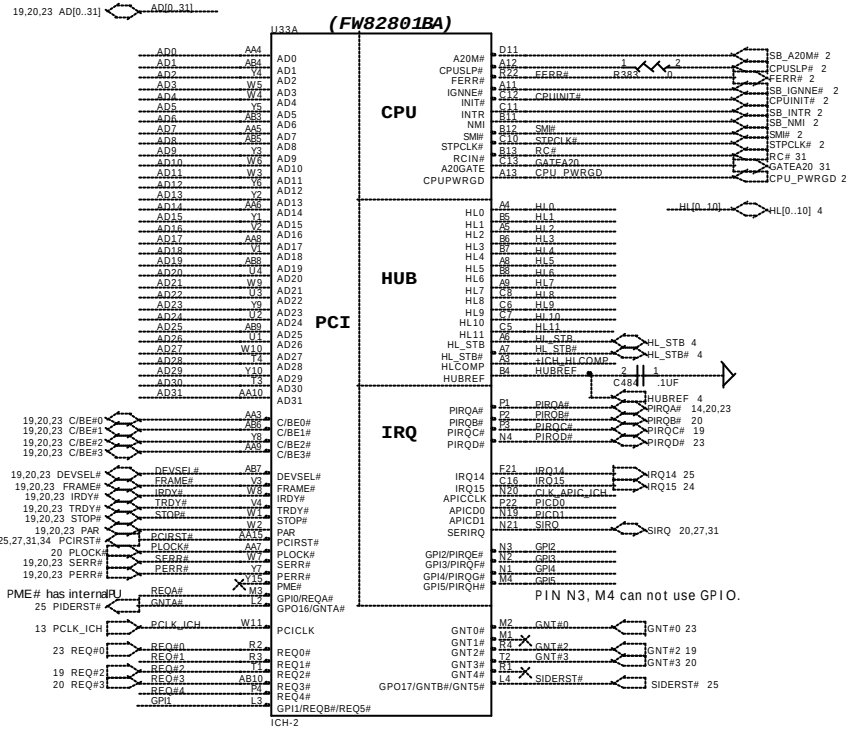
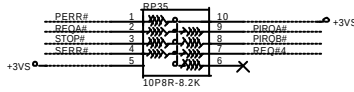
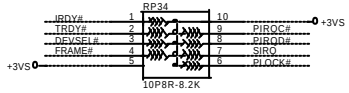
ICH-2

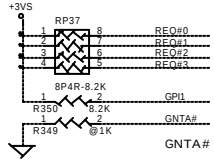


PCI Pullups

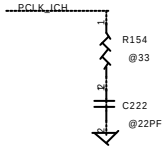


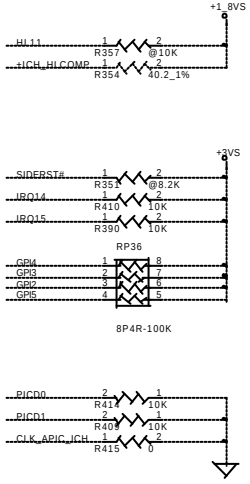


PCI REQ ASSIGMENT	
REQ#0	WLAN
REQ#1	NC
REQ#2	1394
REQ#3	PCMCIA CONTROLLER
REQ#4	NC



GNTA# Strapping for "A16 swap override":"0"->Enable





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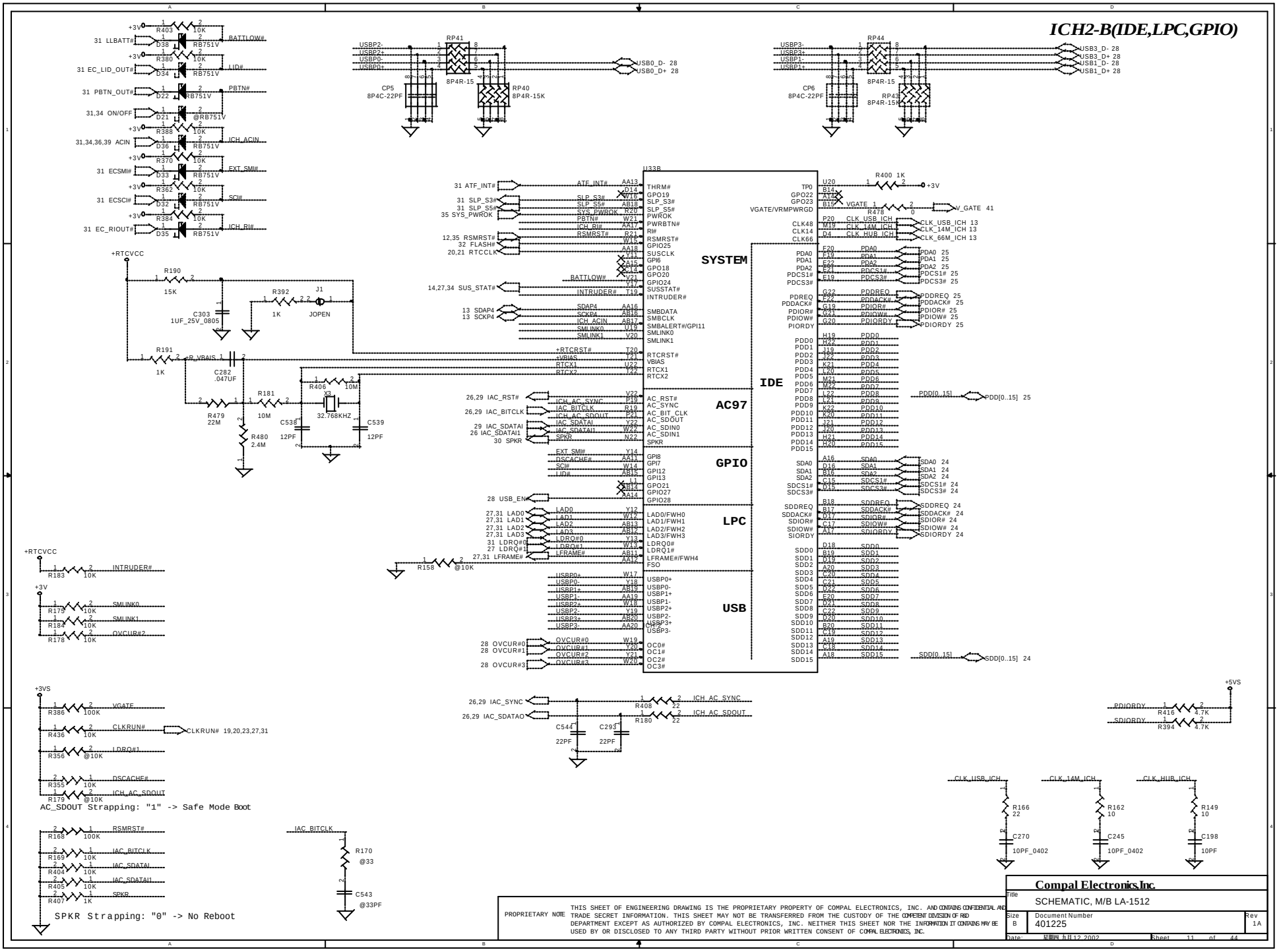
ICH2-B(IDE,LPC,GPIO)



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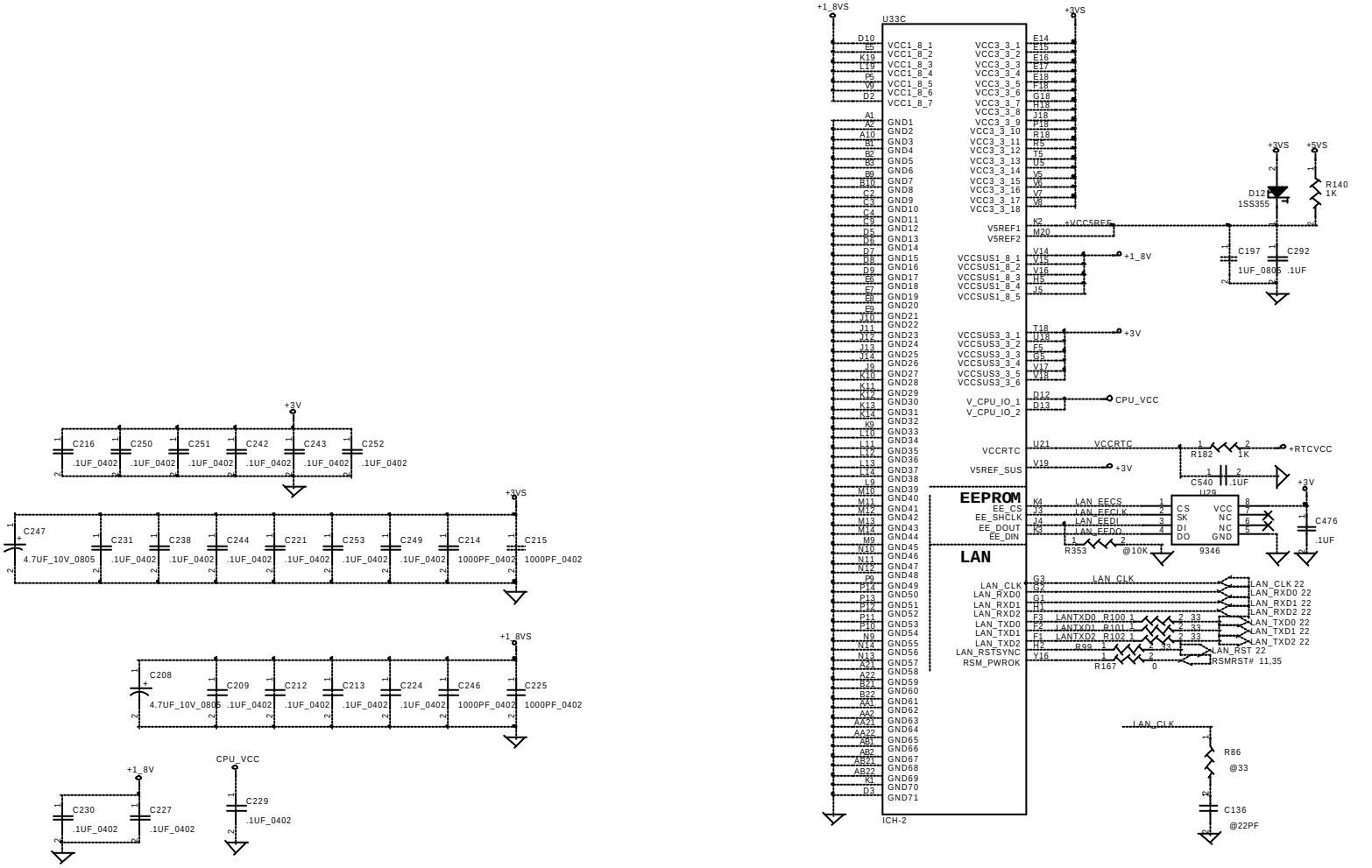
ICH2-C(LAN,Power)



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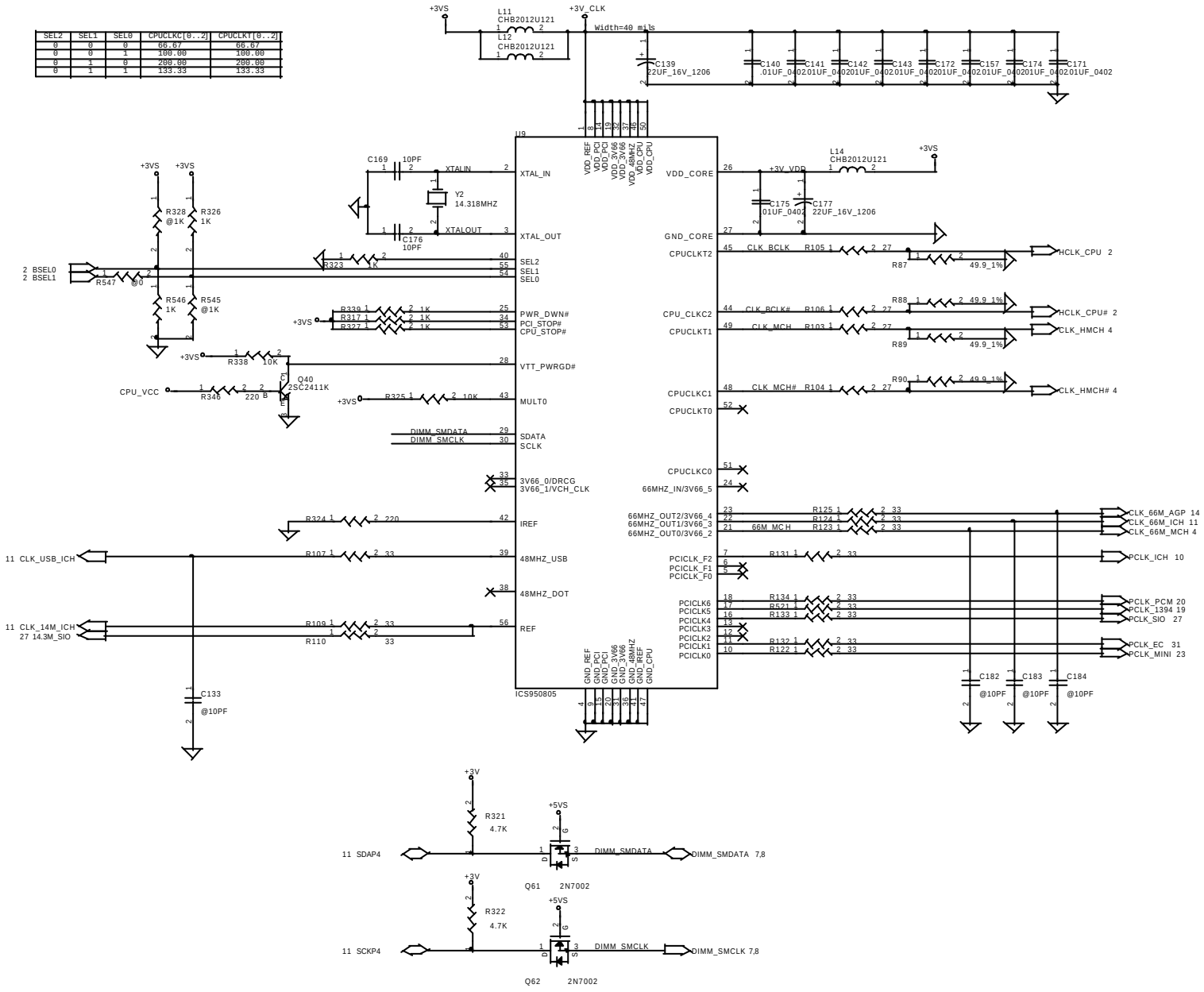
Clock Generator

SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	66.67	66.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33



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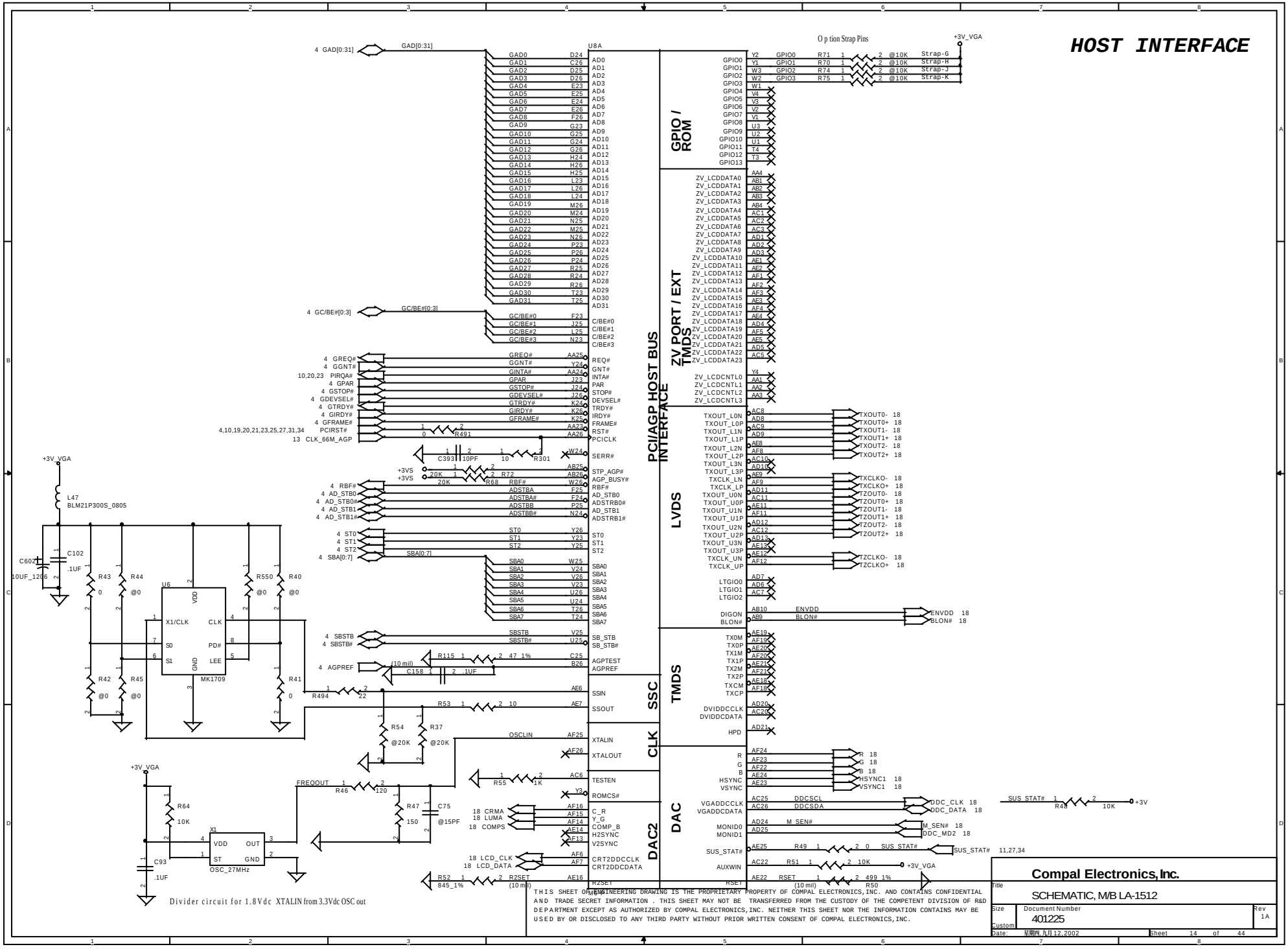
HOST INTERFACE



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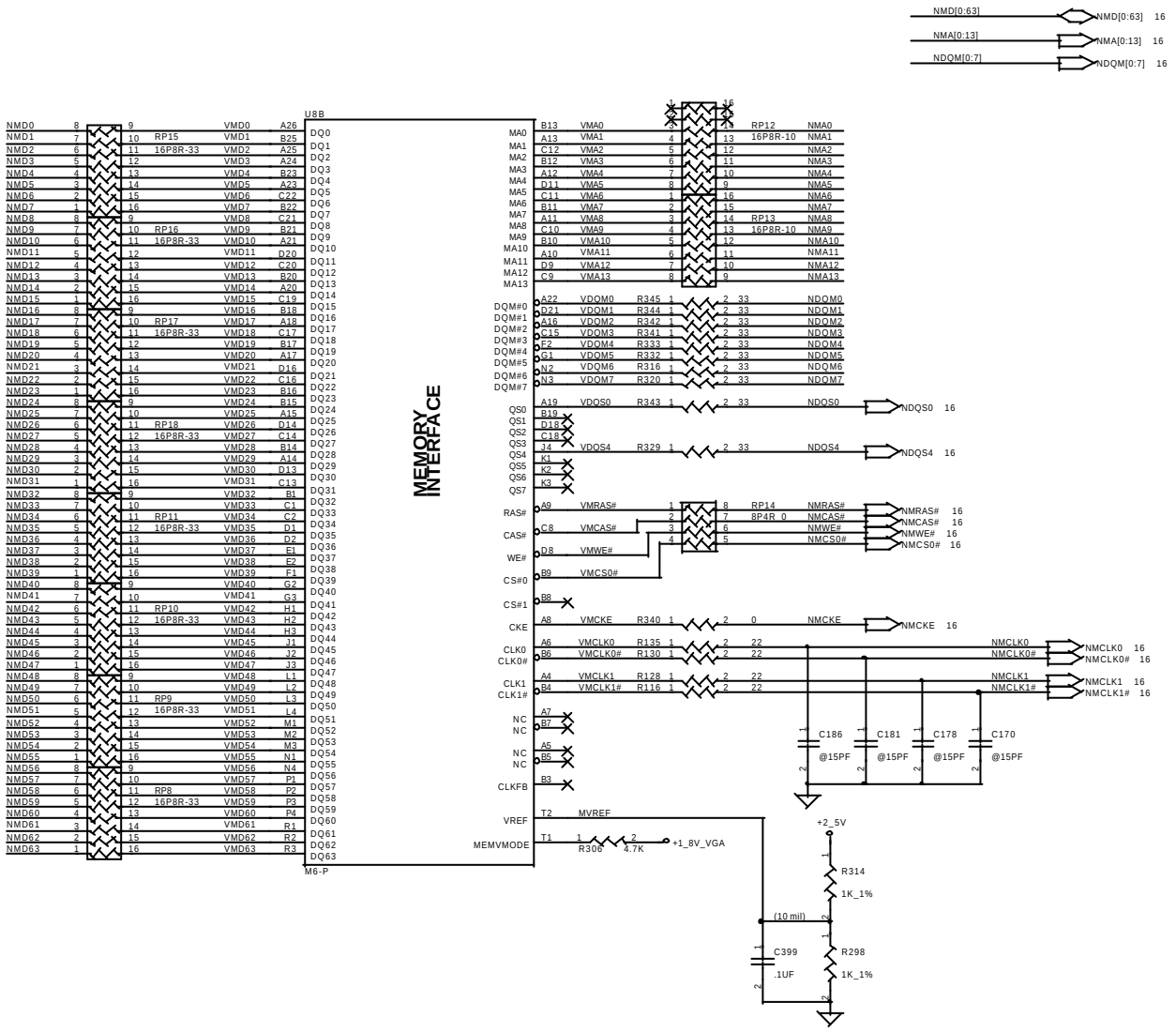
MEMORY INTERFACE



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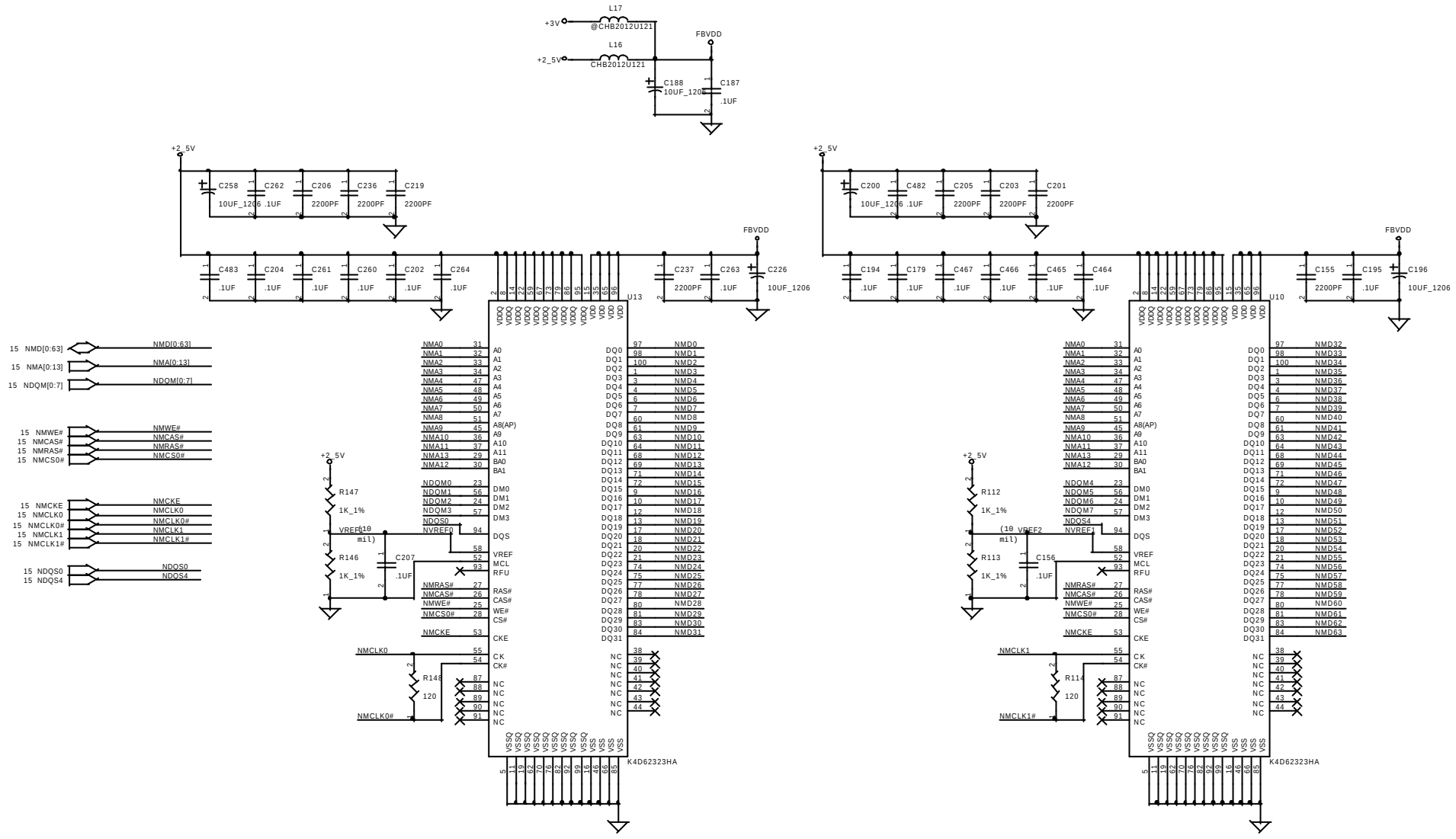
DDR SDRAM



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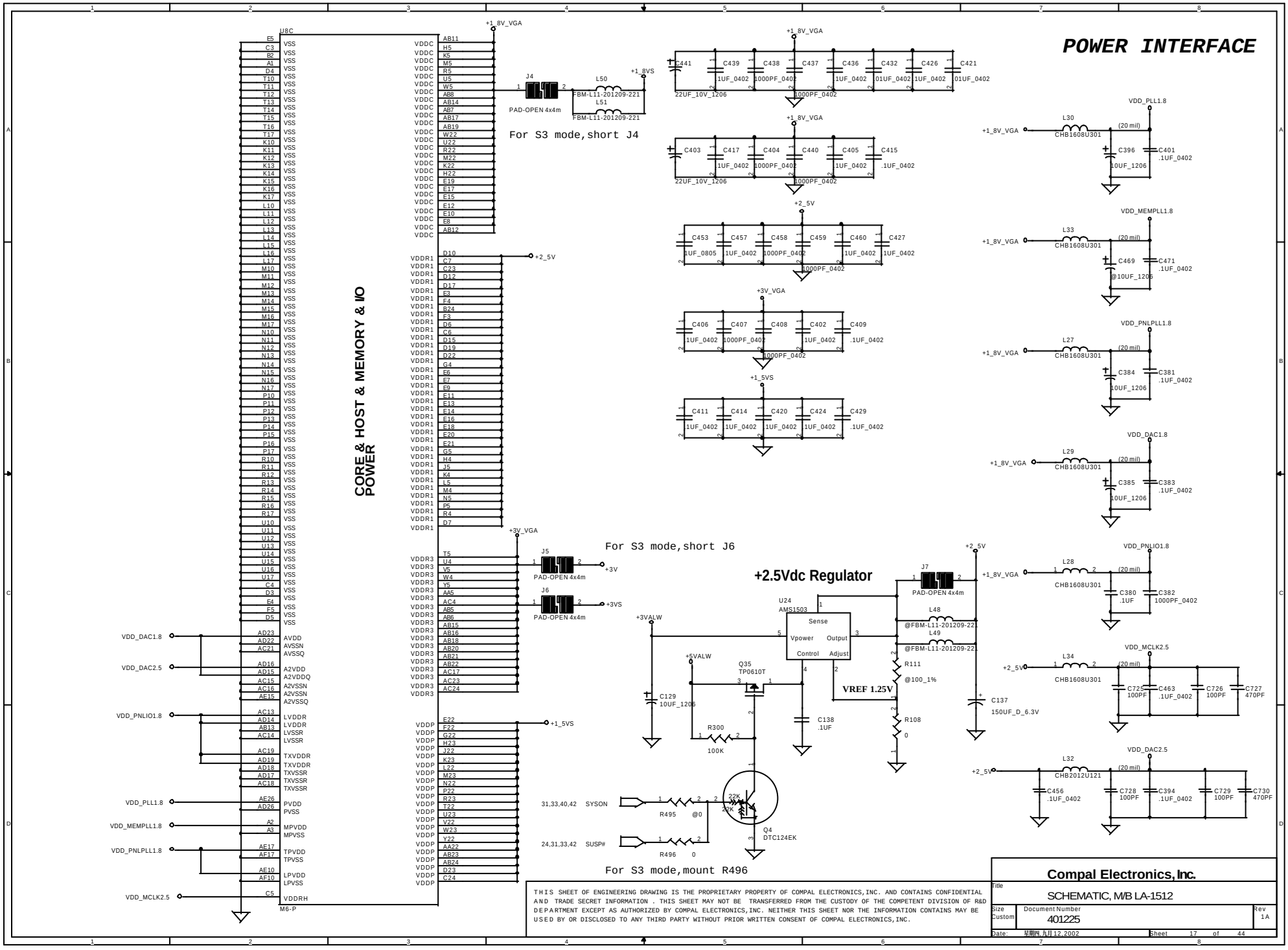
POWER INTERFACE



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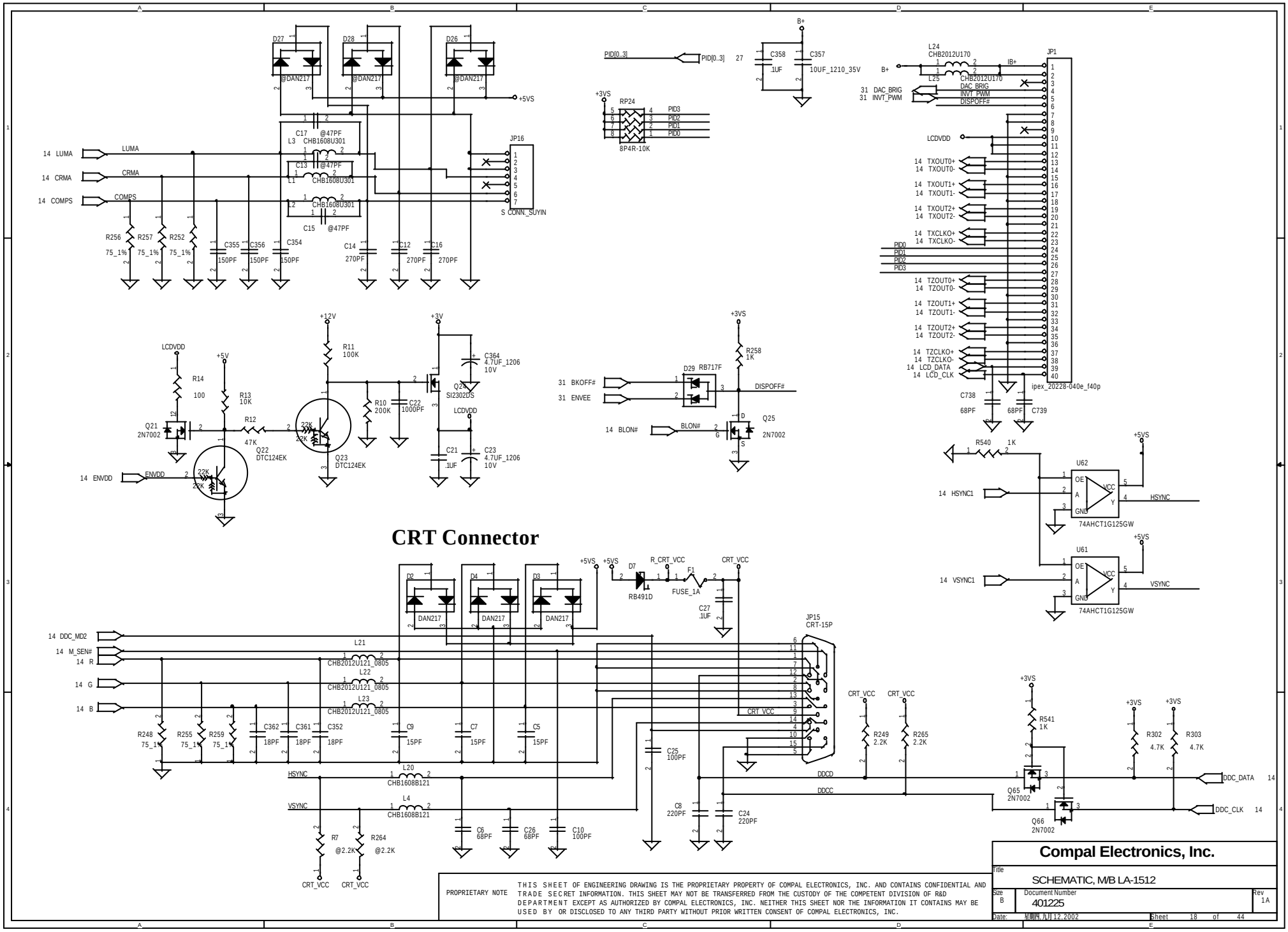
CRT Connector
D27
D28
D26
@DAN217
+5VS
C17 @47PF
L3 CHB1608U301
C13 @47PF
L1 CHB1608U301
L2 CHB1608U301
C15 @47PF
14 LUMA
14 CRMA
14 COMPS
LUMA
CRMA
COMPS
JP16
S CONN_SUYIN
R256 75_1%
R257 75_1%
R252 75_1%
C355 150PF
C356 150PF
C354 150PF
C14 270PF
C12 270PF
C16 270PF
PID[0..3]
27
C358 .1UF
C357 10UF_1210_35V
B+
+3VS
RP24
8P4R-10K
PID3
PID2
PID1
PID0
L24 CHB2012U170
L25 CHB2012U170
IB+
31 DAC_BRIG
31 INVT_PWM
DAC_BRIG
INVT_PWM
DISPOFF#
JP1
LCDVDD
14 TXOUT0+
14 TXOUT0-
14 TXOUT1+
14 TXOUT1-
14 TXOUT2+
14 TXOUT2-
14 TXCLKO+
14 TXCLKO-
14 TZOUT0+
14 TZOUT0-
14 TZOUT1+
14 TZOUT1-
14 TZOUT2+
14 TZOUT2-
14 TZCLKO+
14 TZCLKO-
14 LCD_DATA
14 LCD_CLK
ipex_20228-040e_f40p
C738 68PF
C739 68PF
+12V
+3V
R11 100K
C364 4.7UF_1206 10V
Q24 SI2302DS
R10 200K
C22 1000PF
C21 .1UF
C23 4.7UF_1206 10V
R14 100
R13 10K
Q21 2N7002
R12 47K
Q22 DTC124EK
Q23 DTC124EK
22K
14 ENVDD
ENVDD
+5V
R258 1K
D29 RB717F
31 BKOFF#
31 ENVEE
14 BLON#
BLON#
Q25 2N7002
R540 1K
U62
74AHCT1G125GW
14 HSYNC1
HSYNC
U61
14 VSYNC1
VSYNC
D2
D4
D3
DAN217
+5VS
D7 RB491D
R_CRT_VCC
F1 FUSE_1A
CRT_VCC
C27 .1UF
JP15 CRT-15P
14 DDC_MD2
14 M_SEN#
14 R
14 G
14 B
L21 CHB2012U121_0805
L22 CHB2012U121_0805
L23 CHB2012U121_0805
R248 75_1%
R255 75_1%
R259 75_1%
C362 18PF
C361 18PF
C352 18PF
C9 15PF
C7 15PF
C5 15PF
C25 100PF
HSYNC
L20 CHB1608B121
VSYNC
L4 CHB1608B121
R7 @2.2K
R264 @2.2K
C6 68PF
C26 68PF
C10 100PF
C8 220PF
C24 220PF
DDCD
DDCC
R249 2.2K
R265 2.2K
R541 1K
Q65 2N7002
Q66 2N7002
R302 4.7K
R303 4.7K
DDC_DATA
DDC_CLK
14
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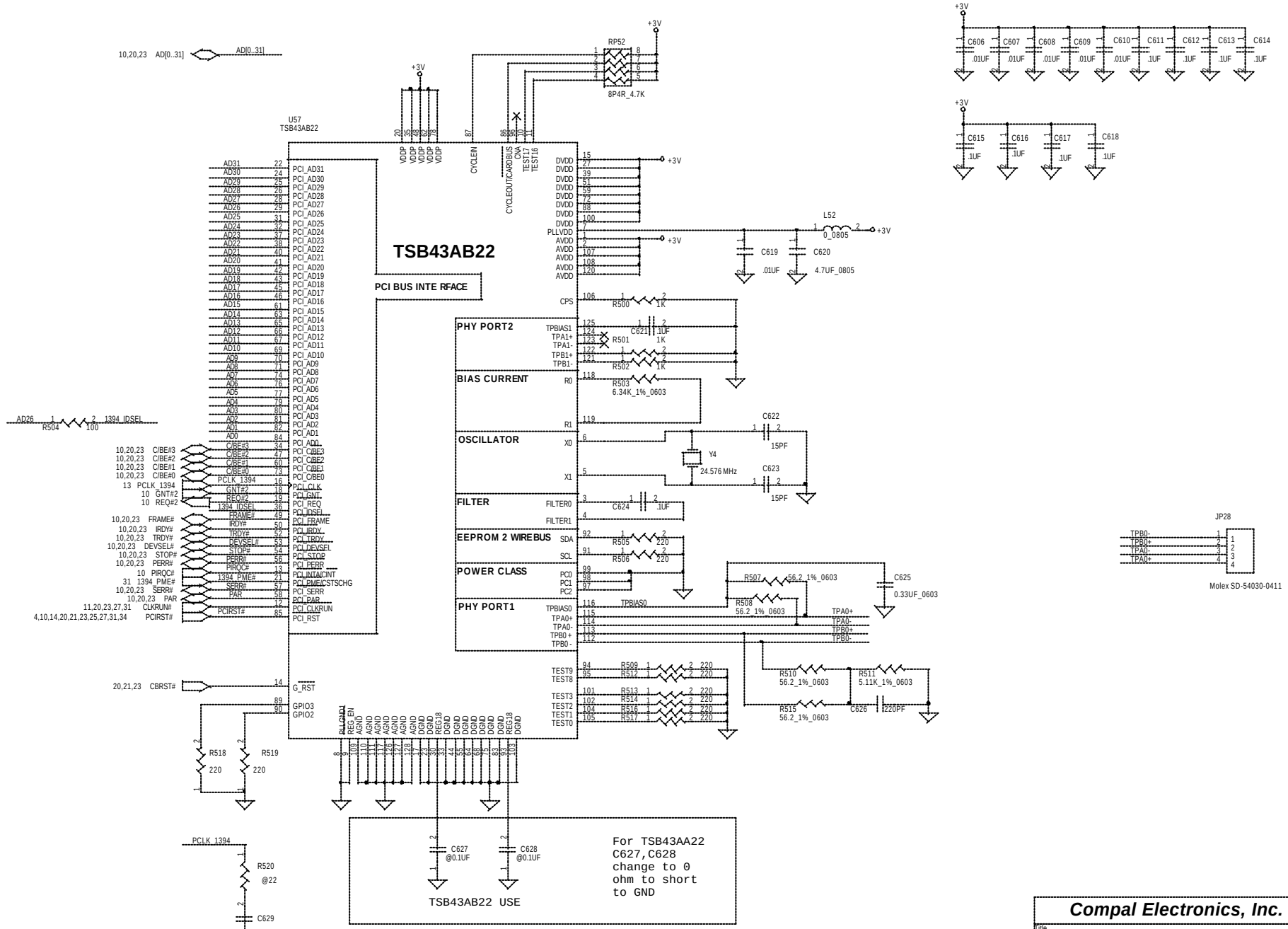

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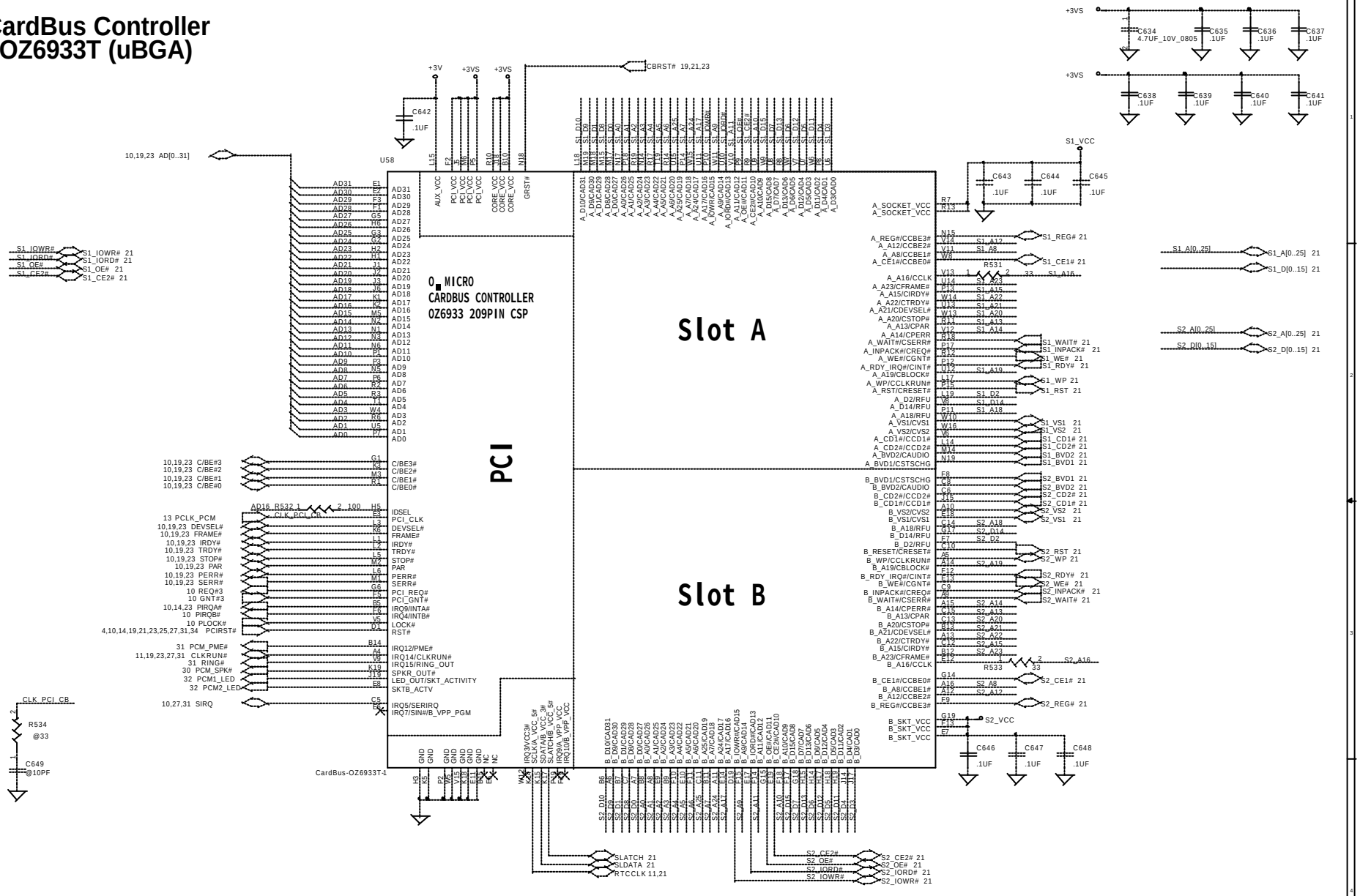
CardBus Controller
OZ6933T (uBGA)



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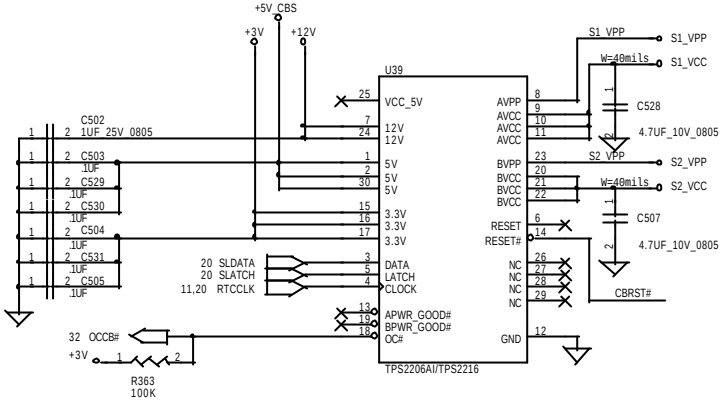
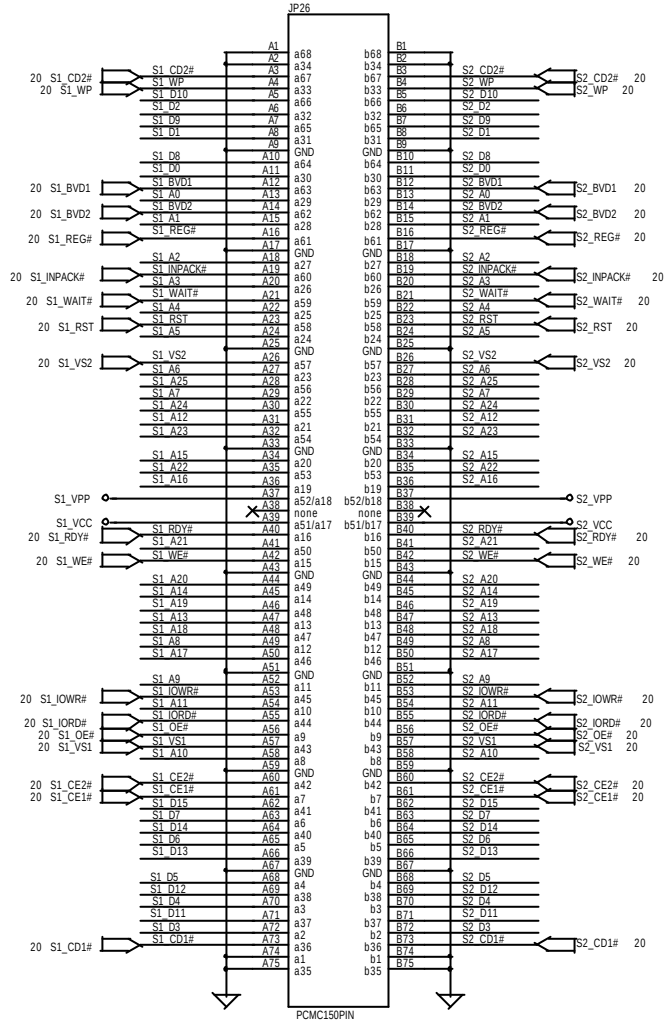
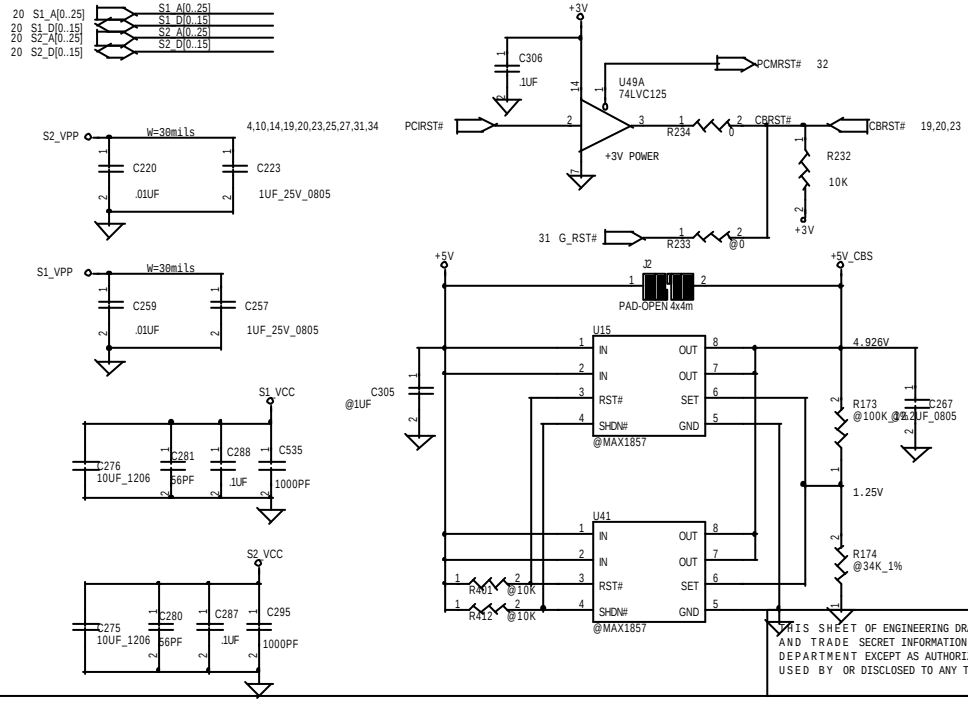
PCMCIA POWER CTRL.

CARDBUS SOCKET







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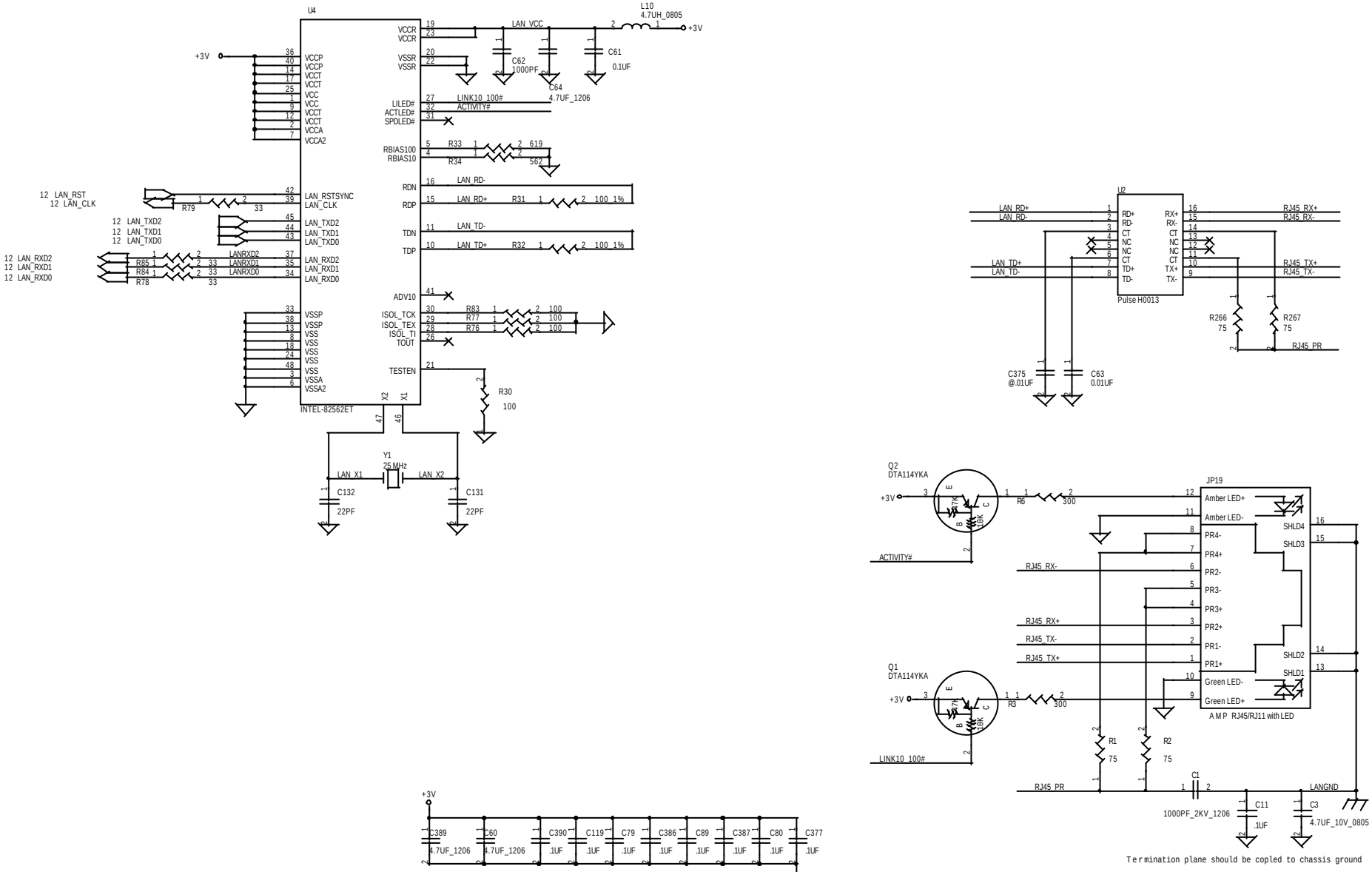

Termination plane should be copled to chassis ground

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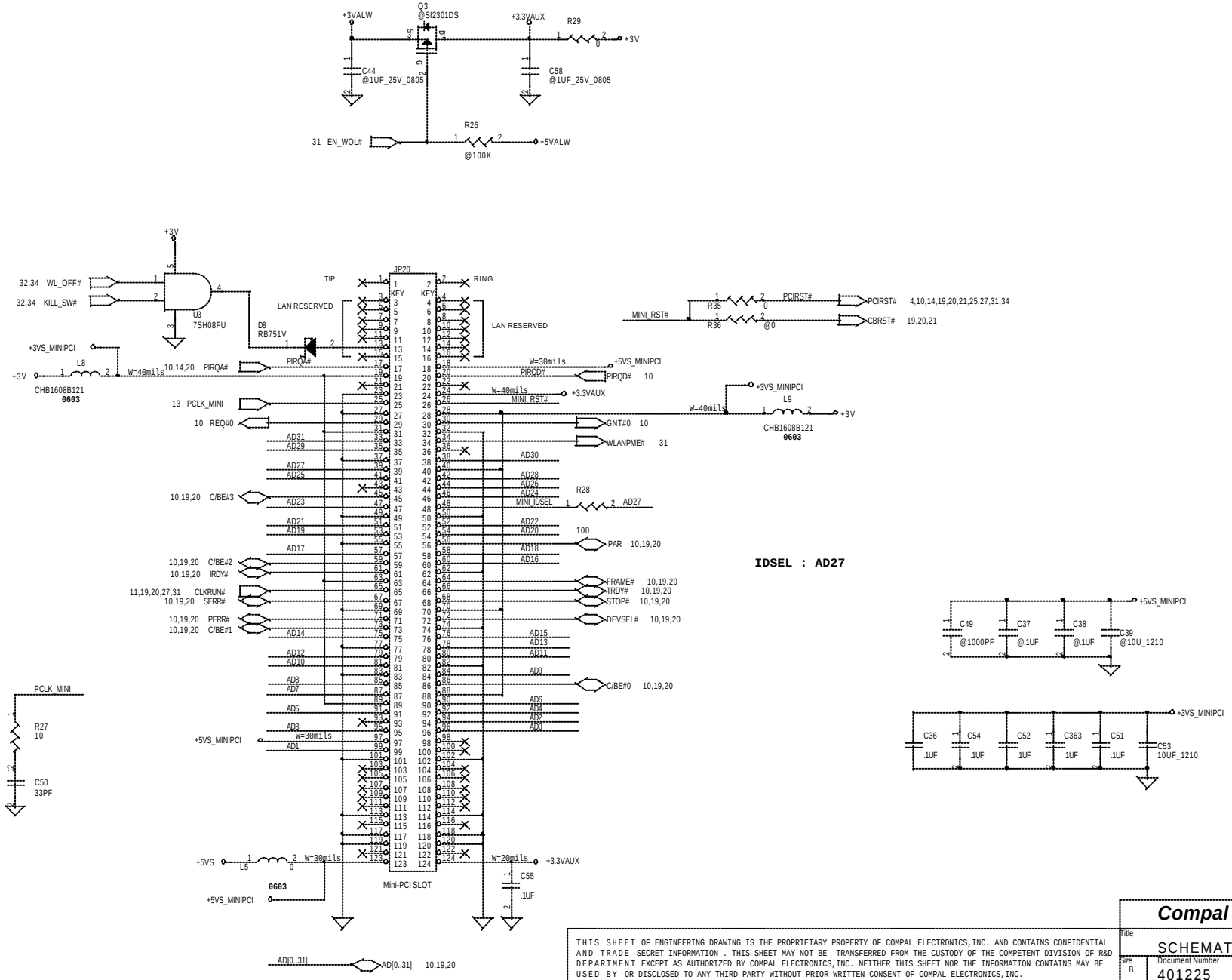

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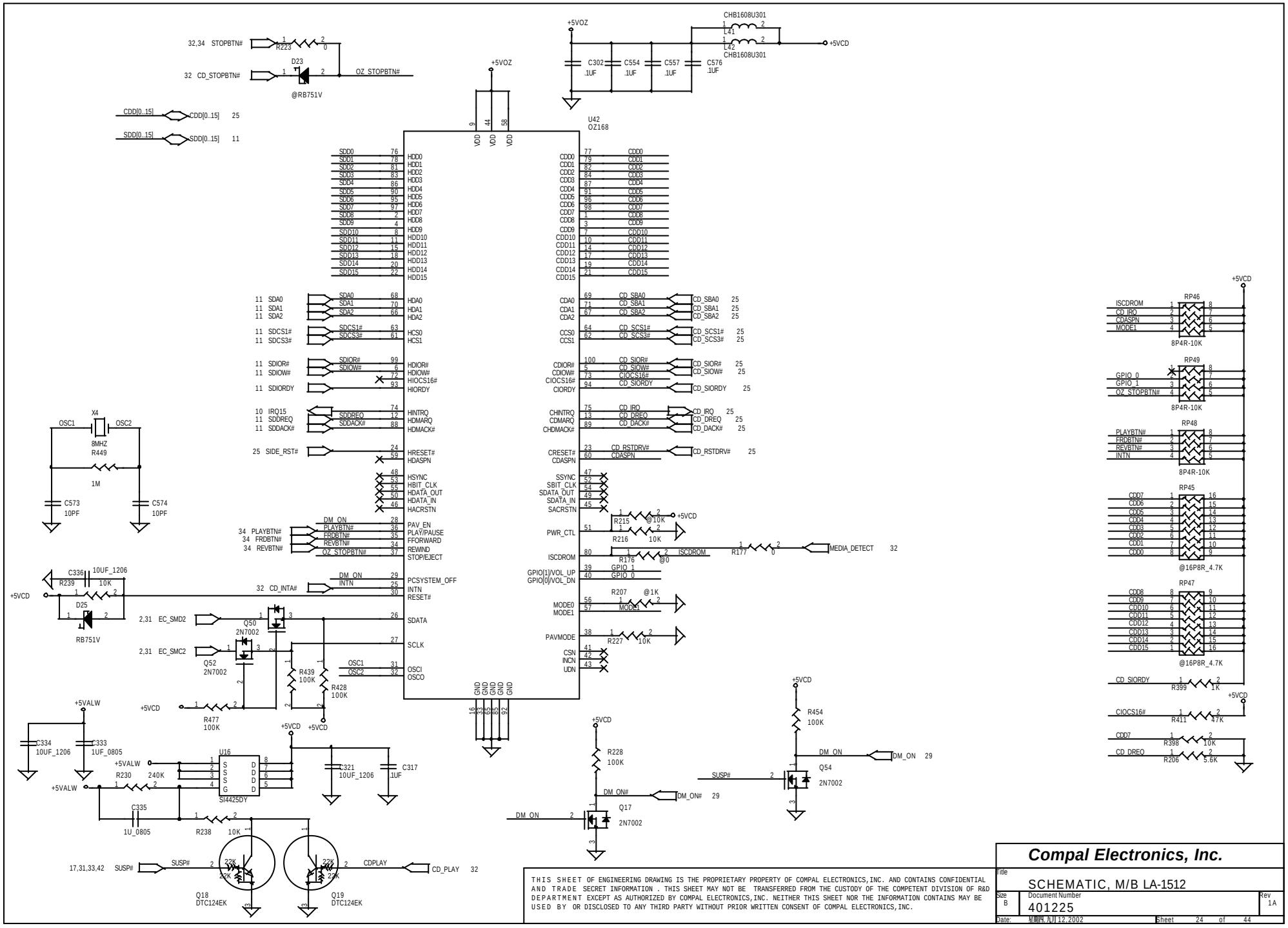

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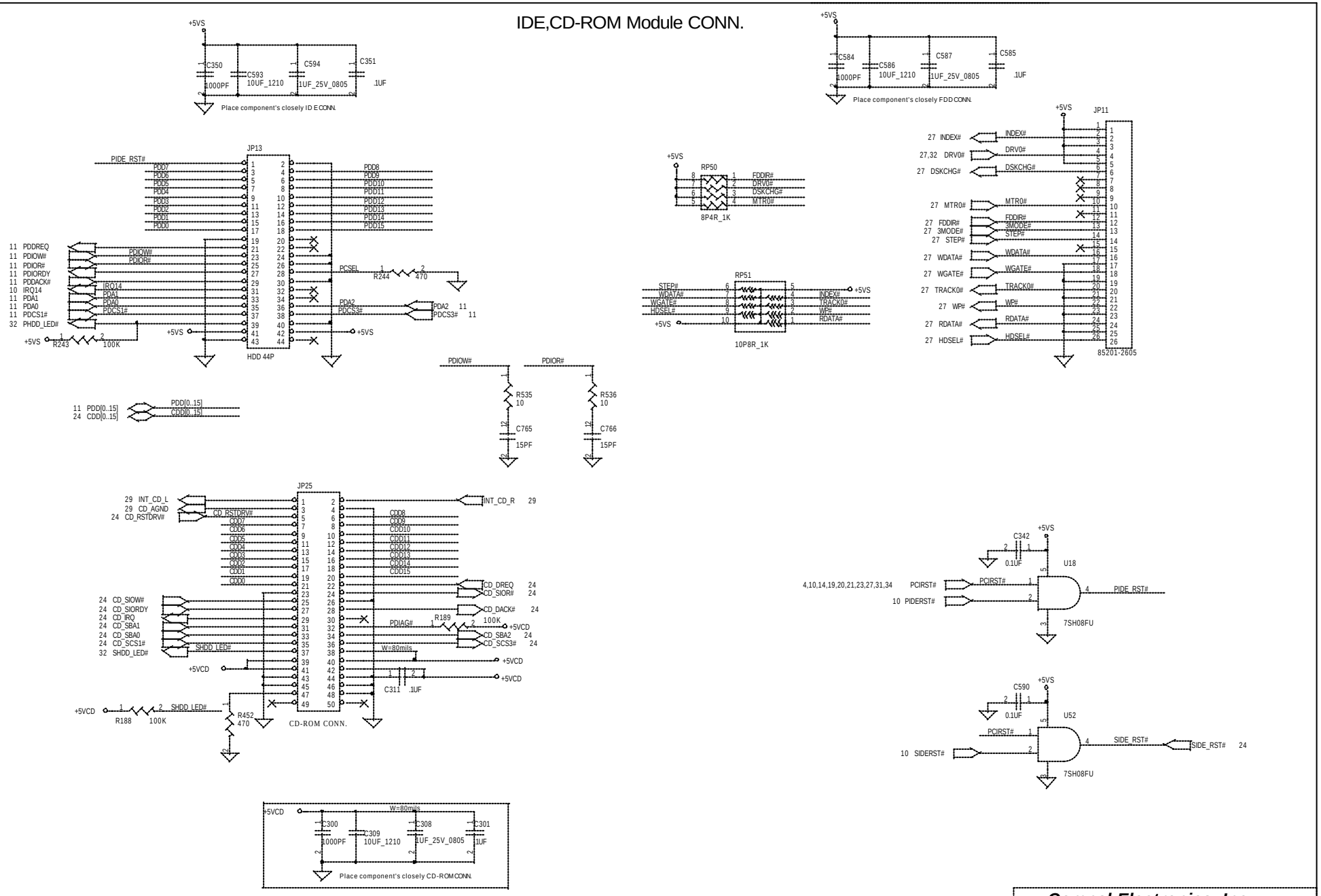
IDE,CD-ROM Module CONN.



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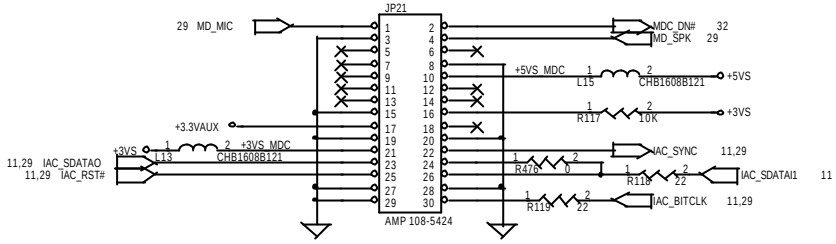
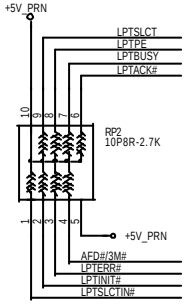
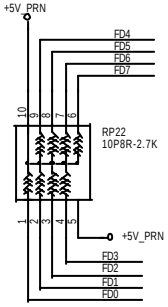
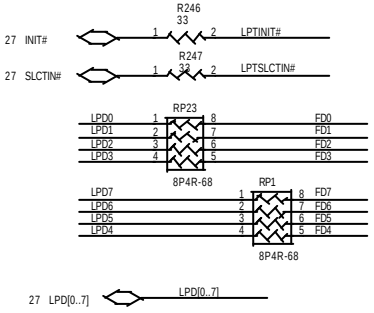
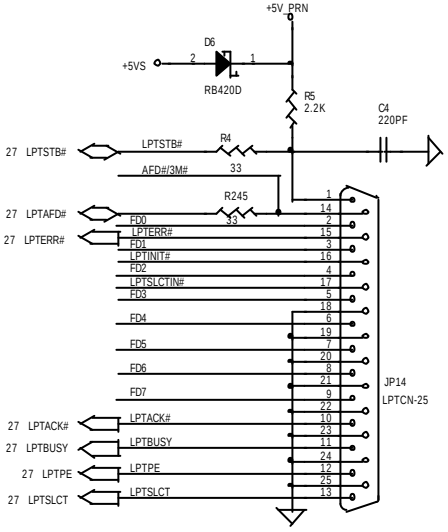


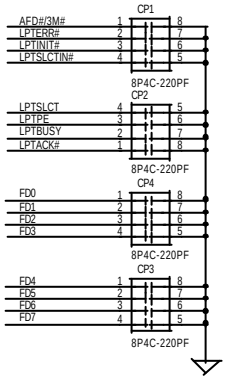
PARALLEL PORT











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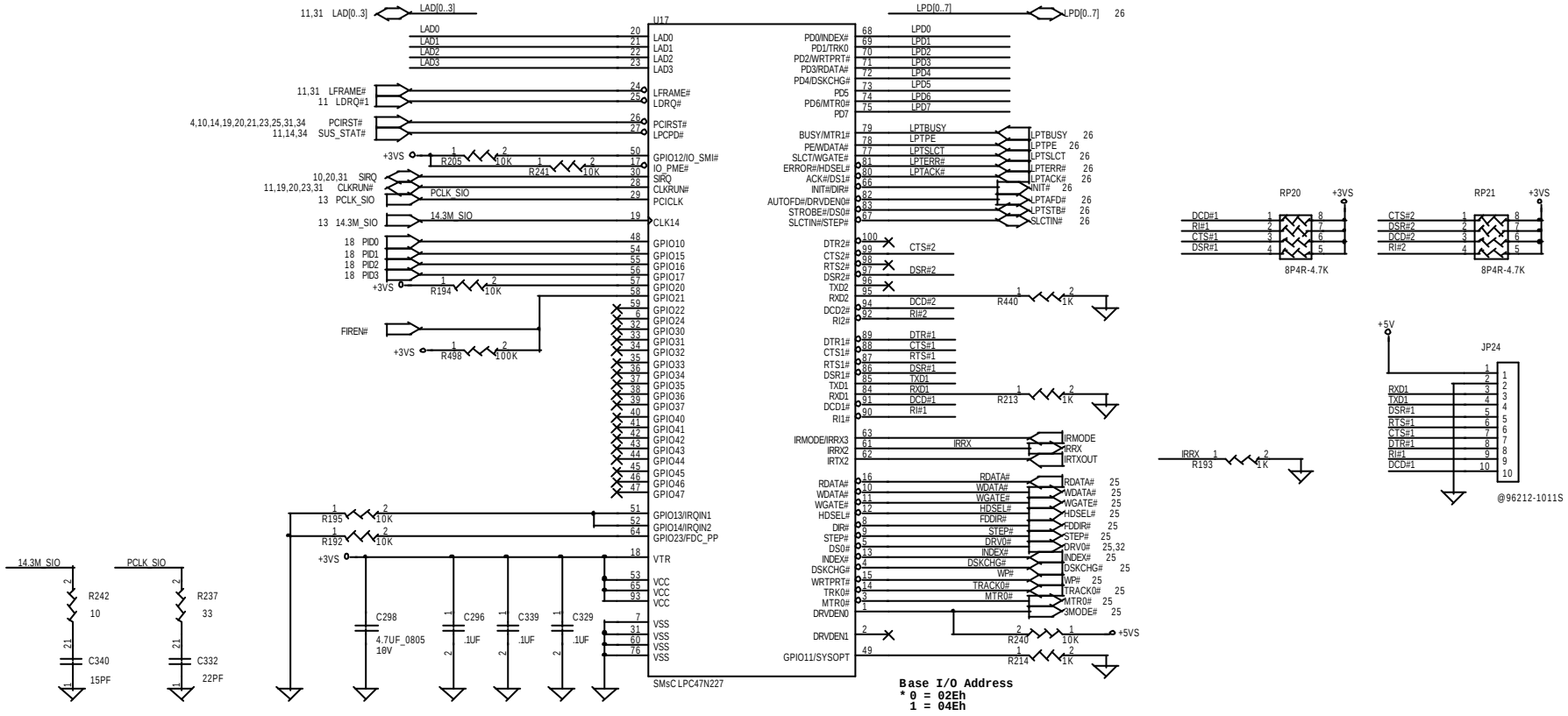
SUPER I/O SMsC FDC47N227



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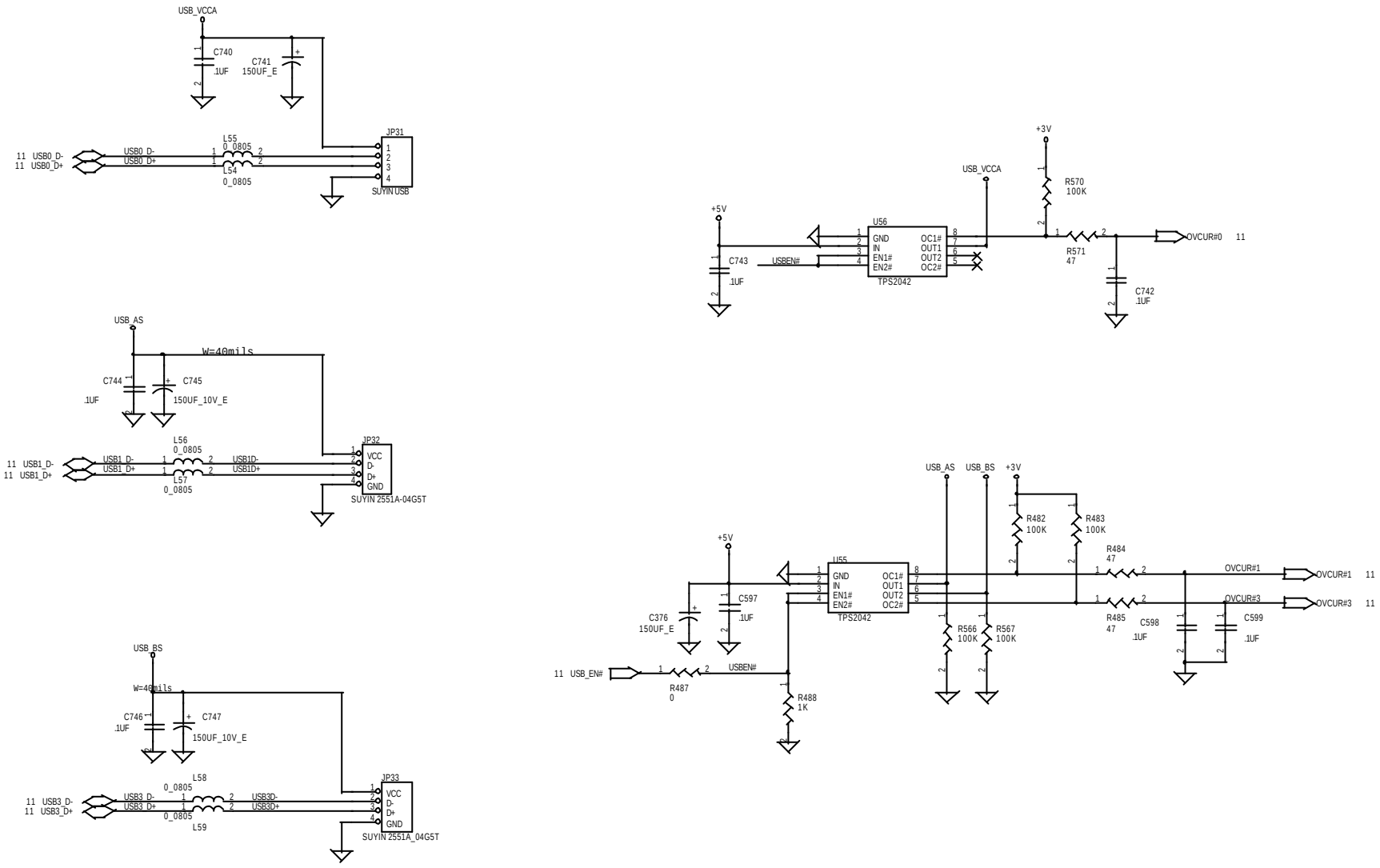

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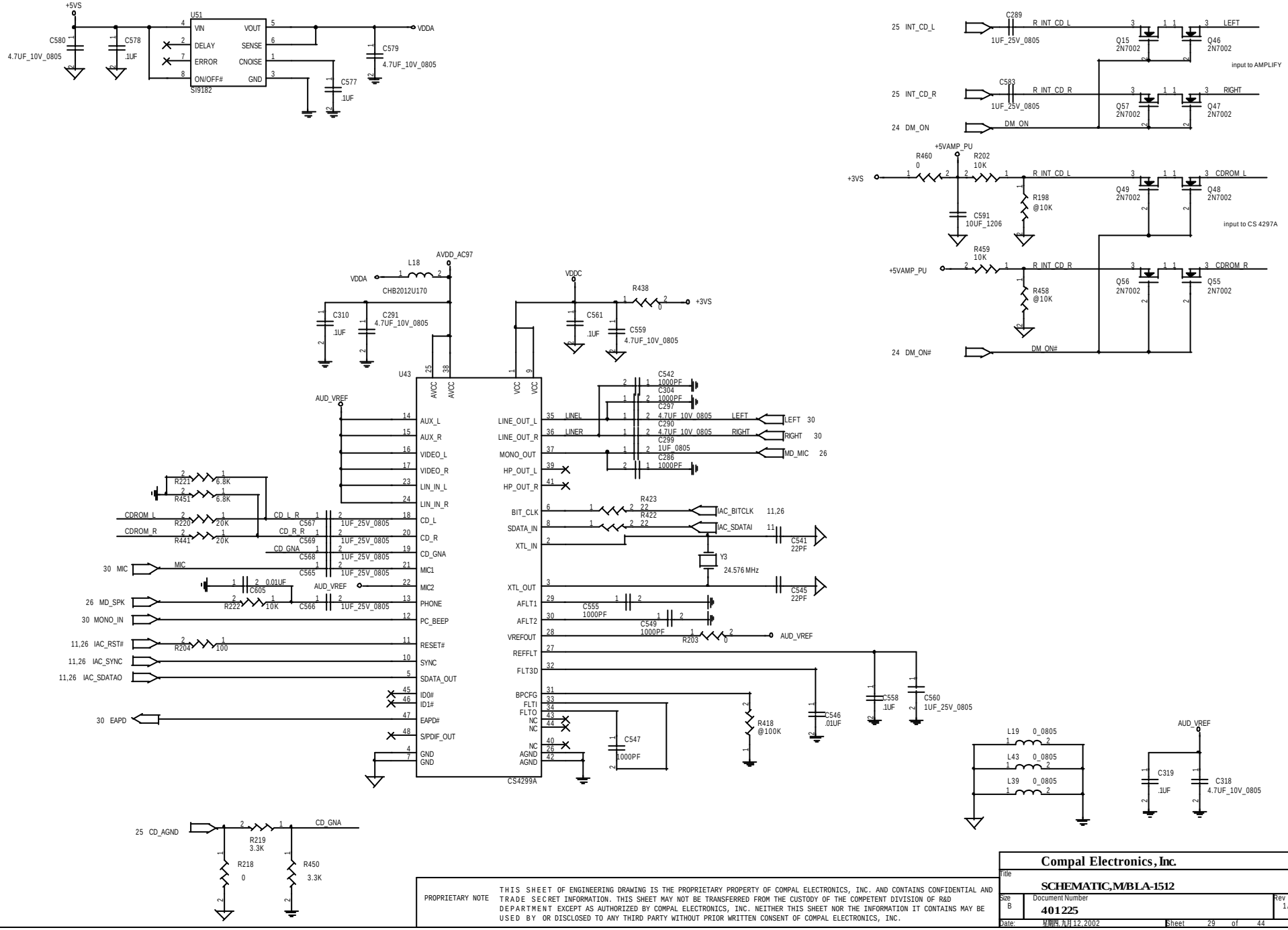
AC97 Codec



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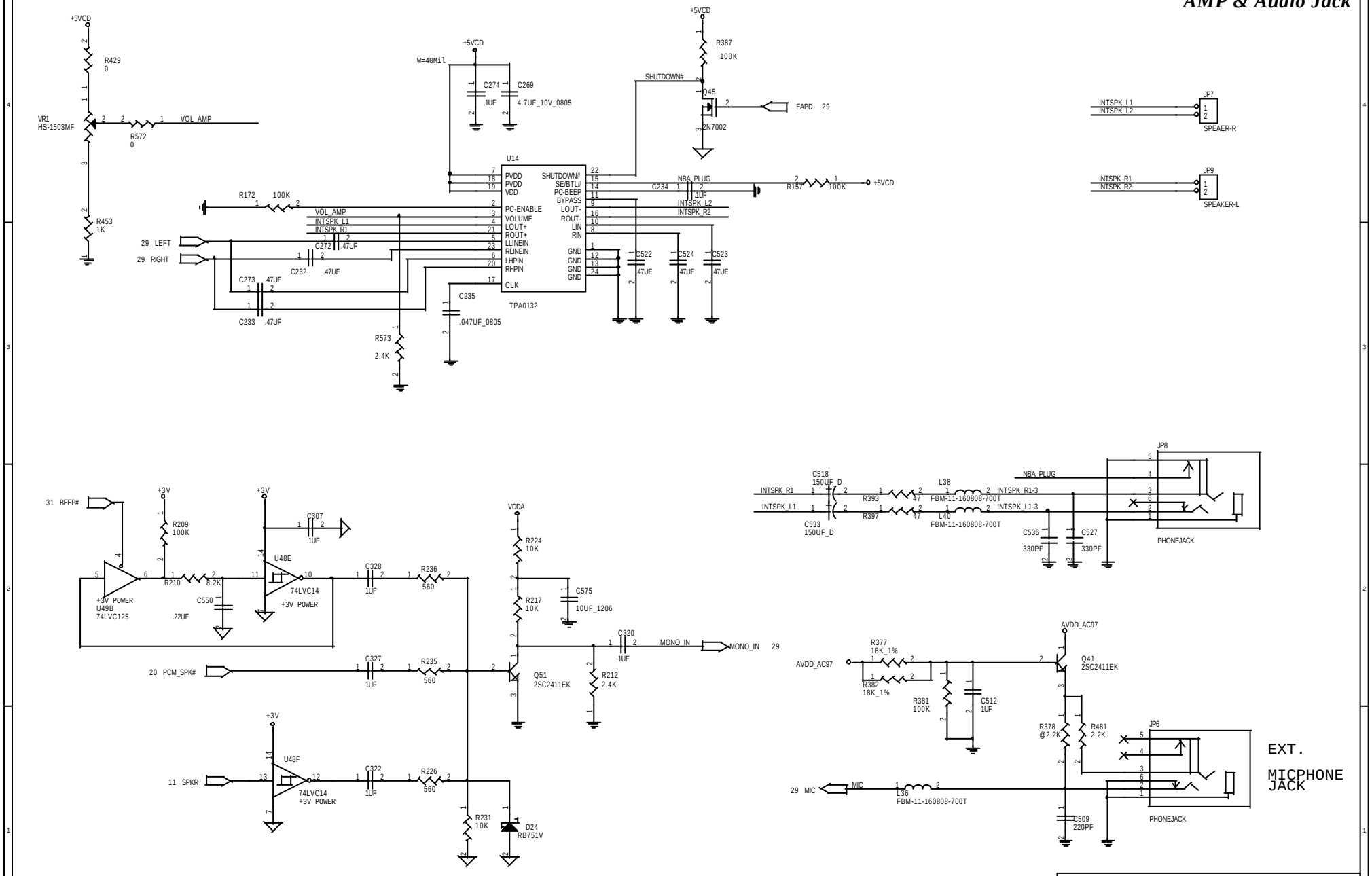
AMP & Audio Jack



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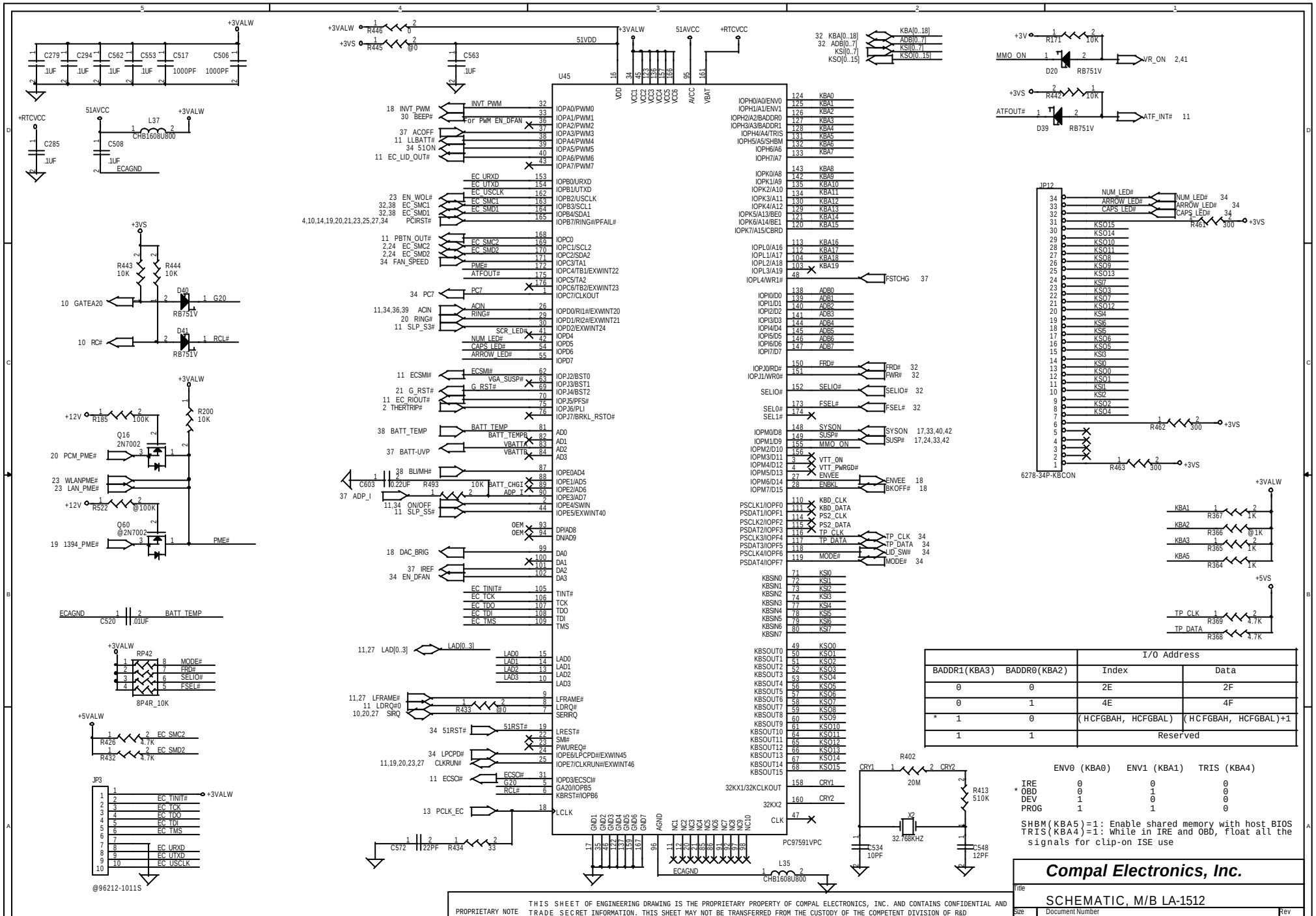

	I/O Address	
BADDR1(KBA3) BADDR0(KBA2)	Index	Data
0 0	2E	2F
0 1	4E	4F
* 1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

	ENV0 (KBA0)	ENV1 (KBA1)	TRIS (KBA4)
IRE	0	0	0
* OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

SHBM(KBA5)=1: Enable shared memory with host BIOS
TRIS(KBA4)=1: While in IRE and OBD, float all the signals for clip-on ISE use

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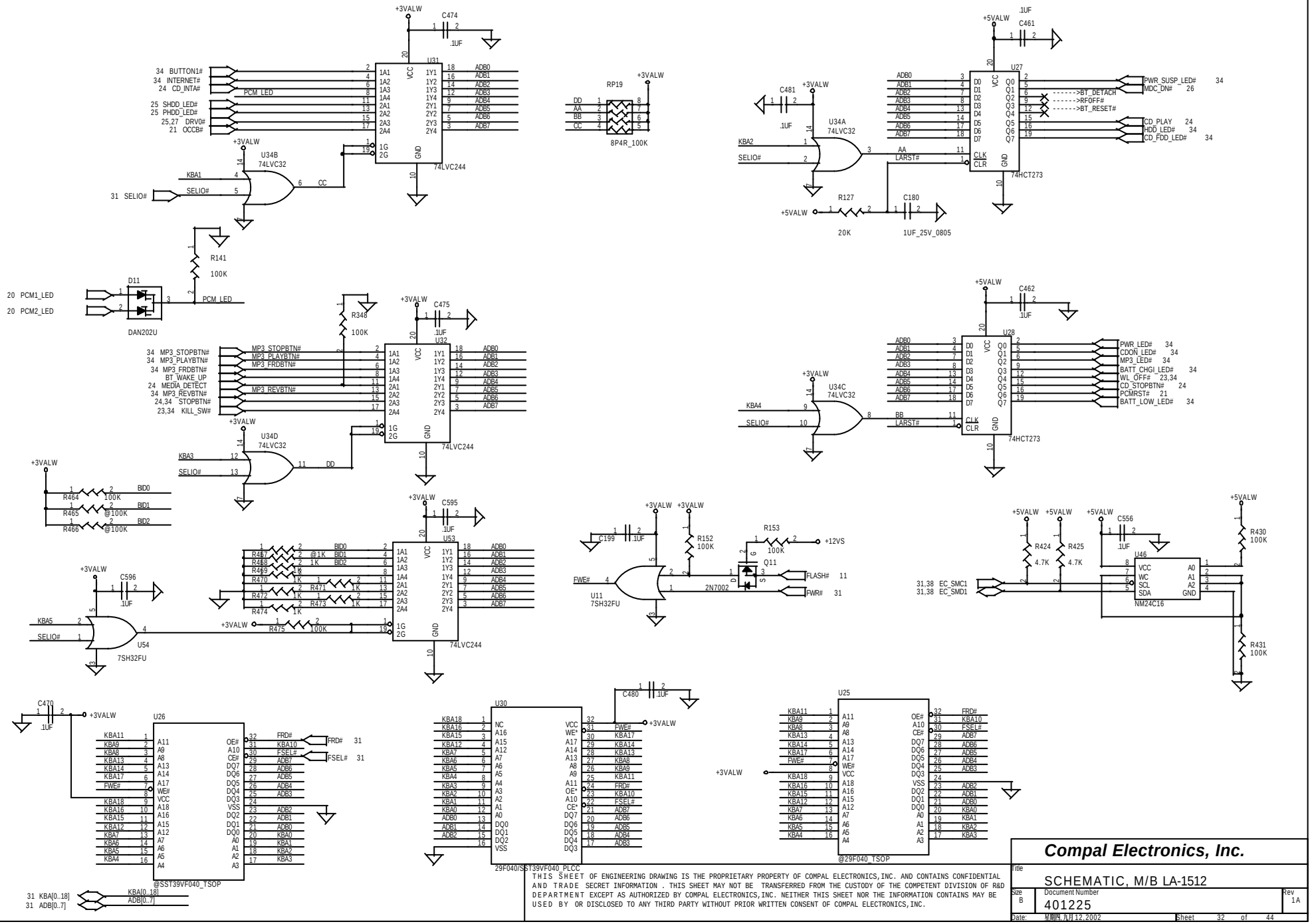

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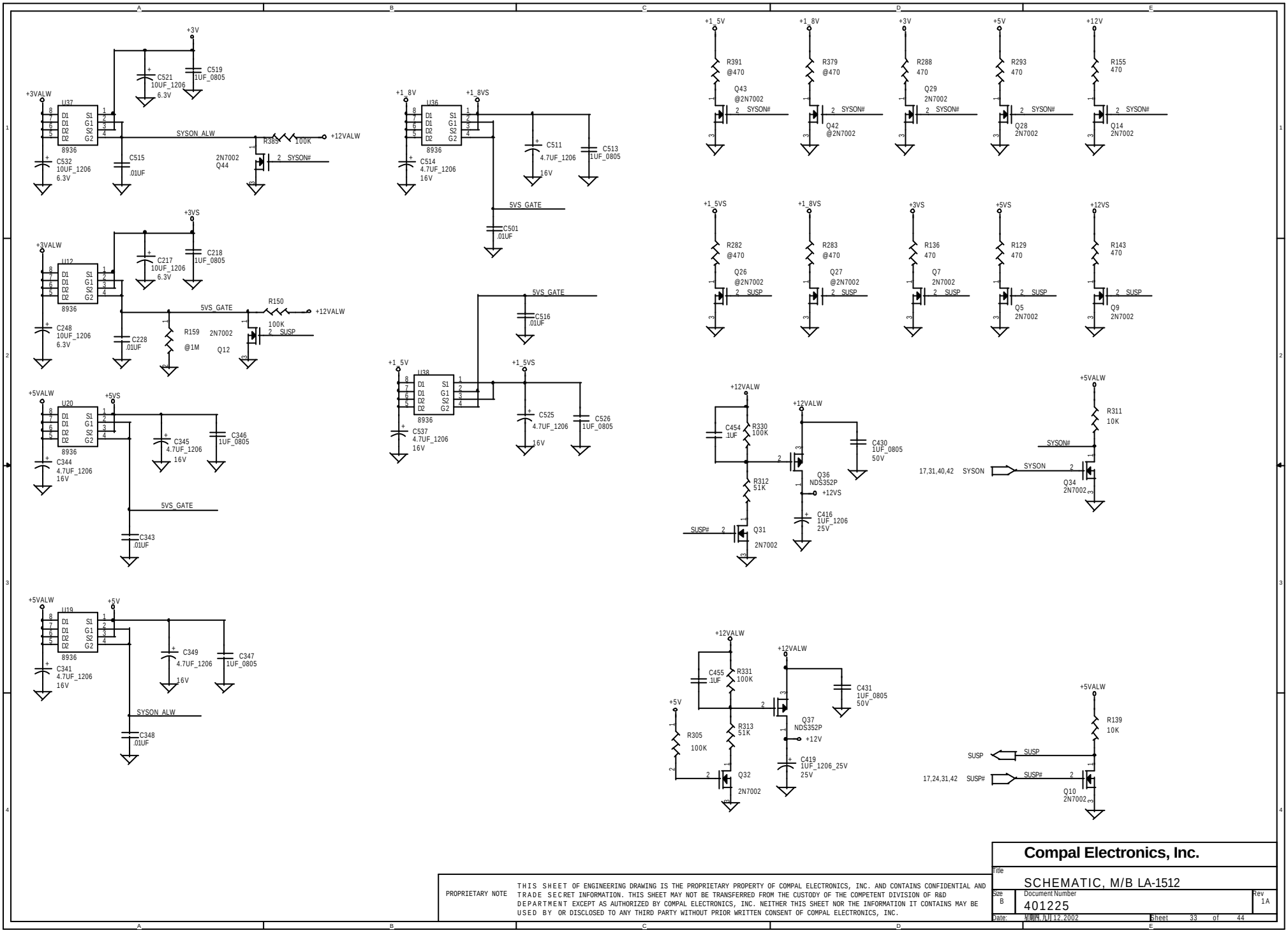

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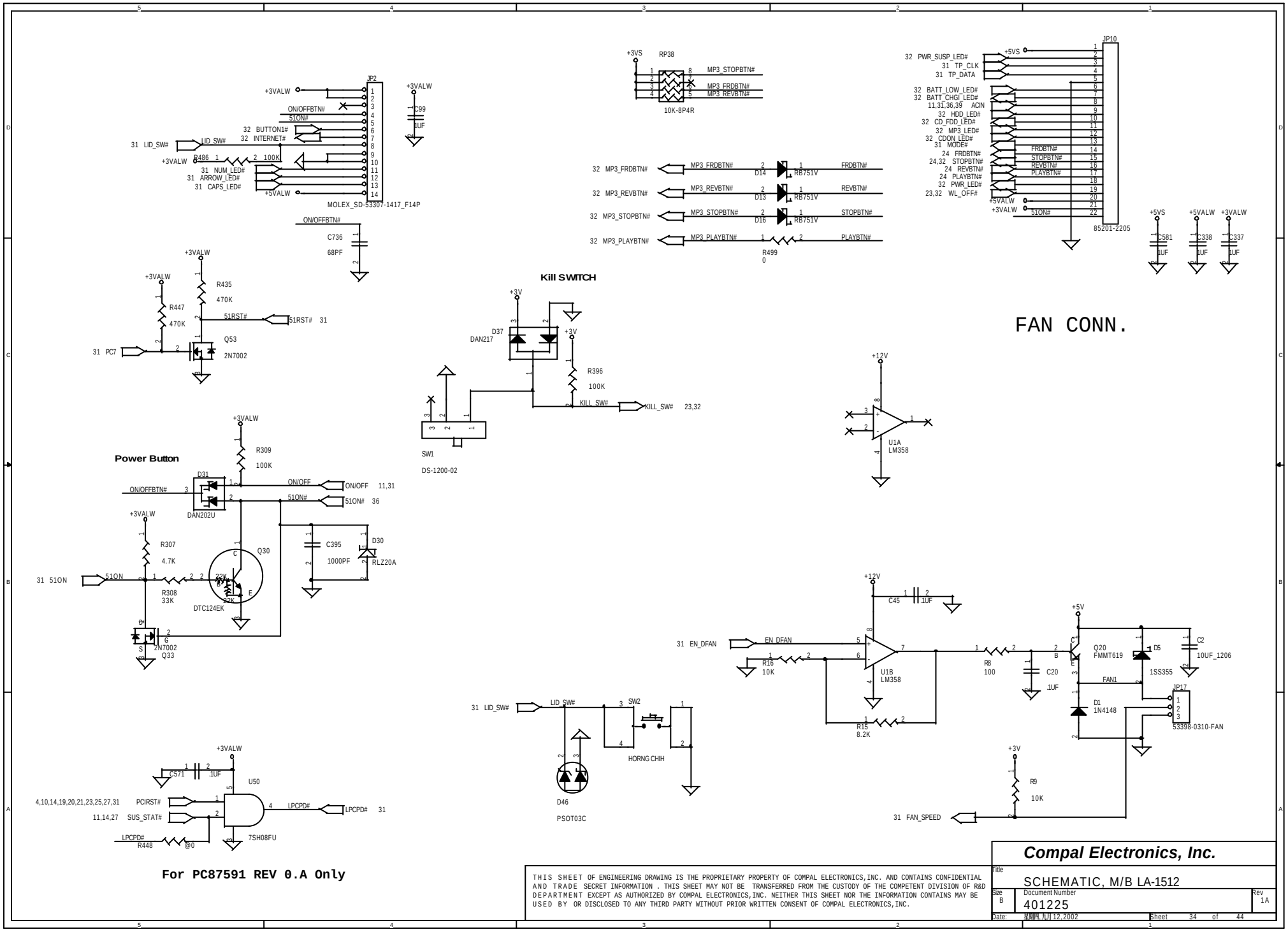

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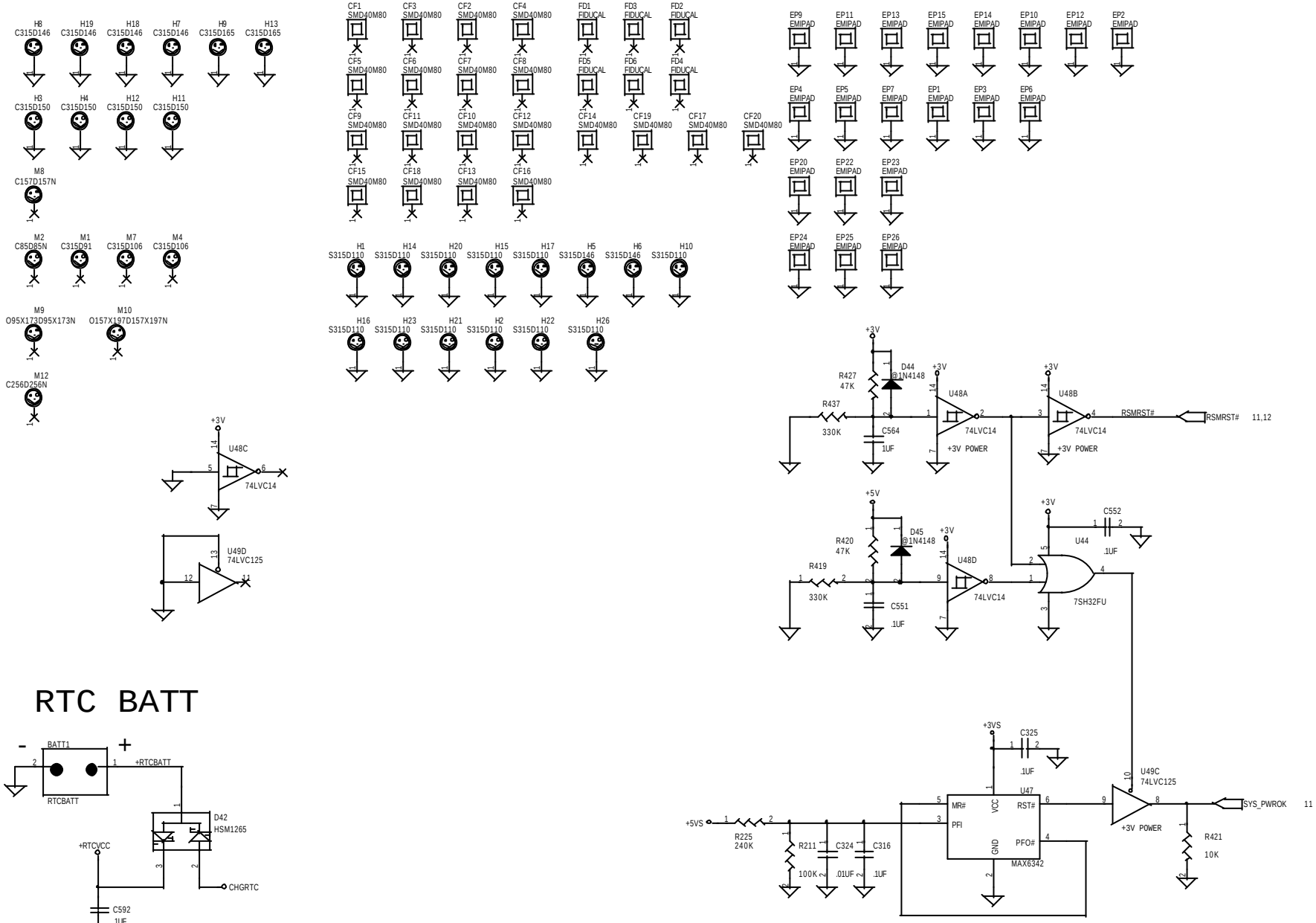

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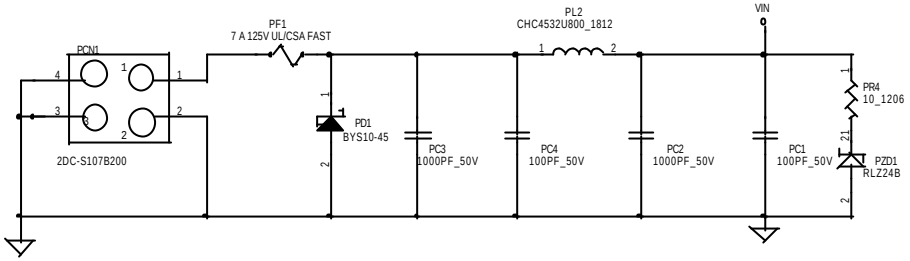
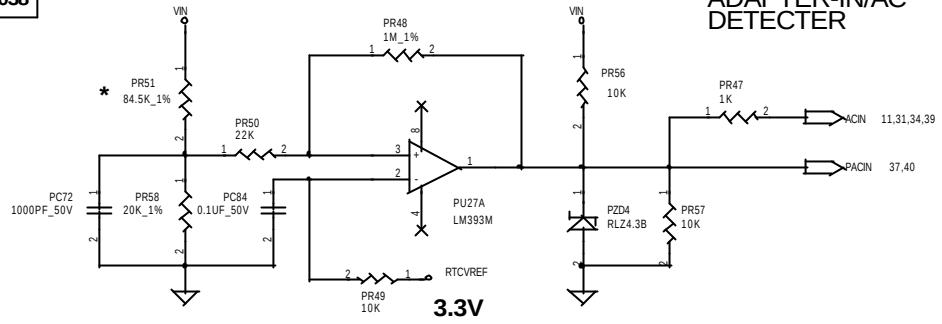
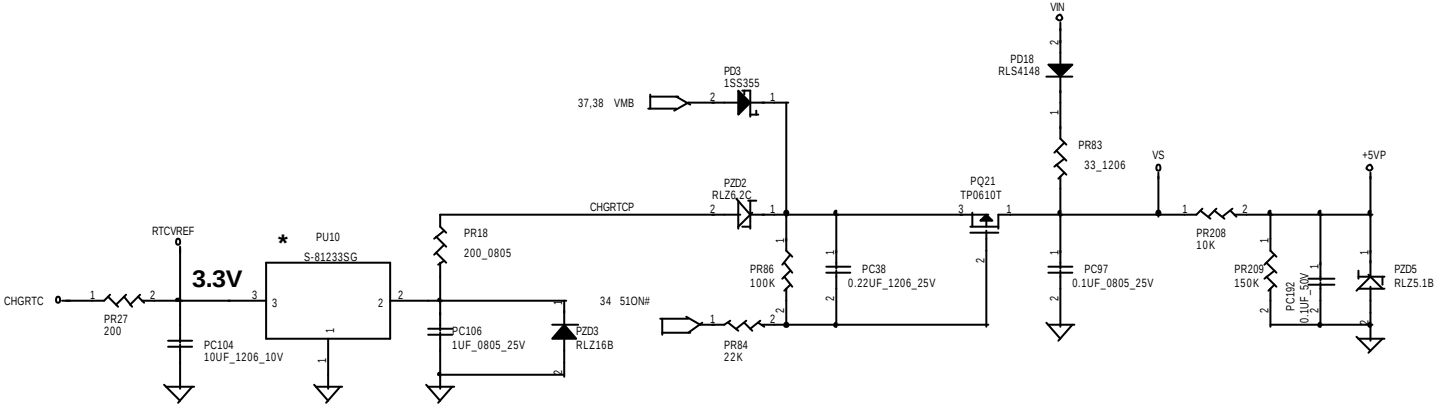
Vin Detector

High	**18.764**	**17.901**	**17.063**
Low	**17.745**	**16.903**	**16.038**

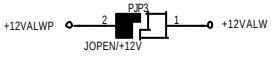


ADAPTER-IN/AC DETECTER





(3A,120mils ,Via NO.= 6)



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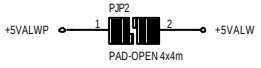

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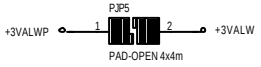

(5A,200mils ,Via NO.= 10)

(3A,120mils ,Via NO.= 6)

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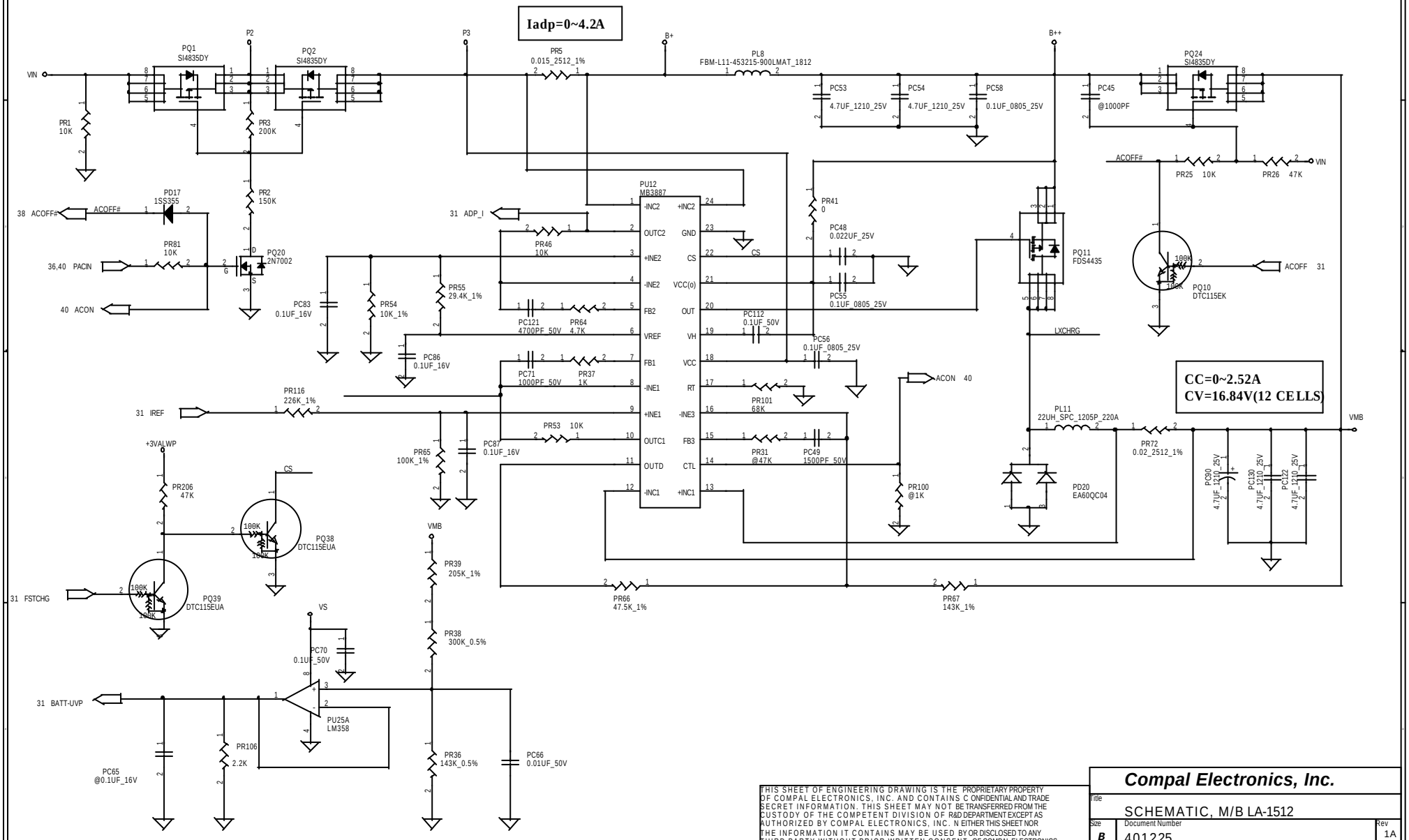
CHARGER



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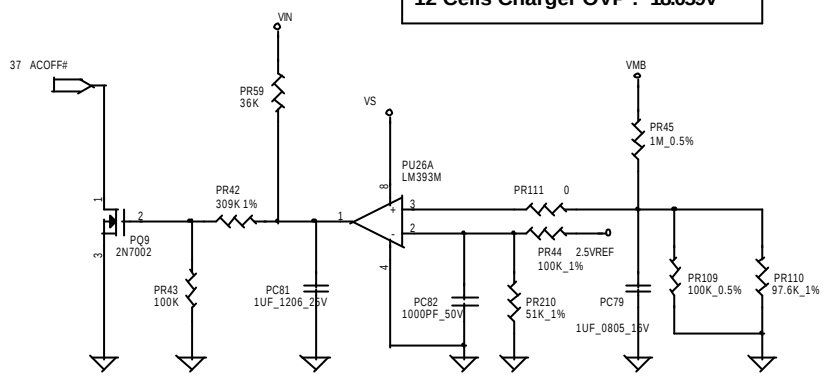
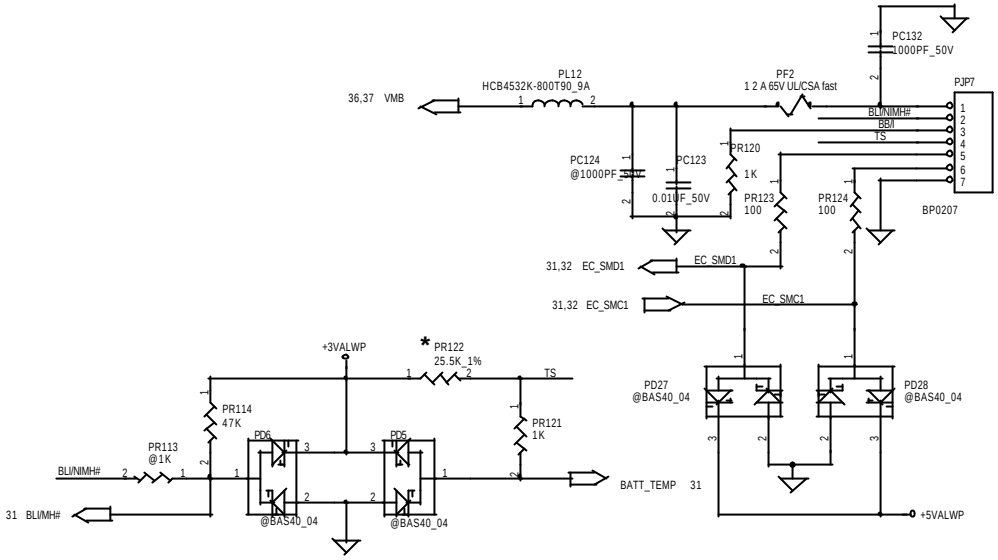
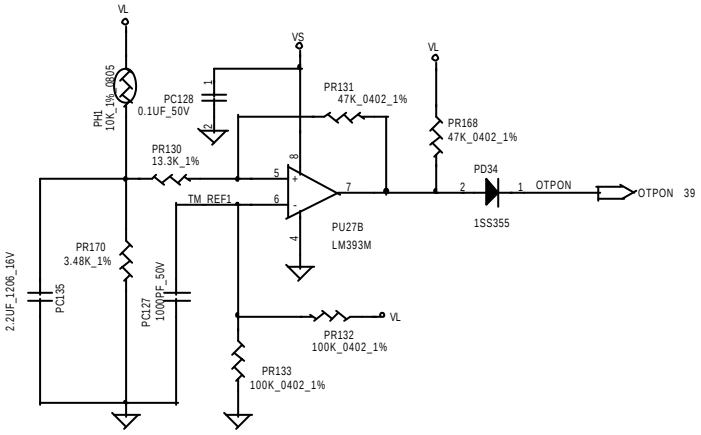
12 Cells Charger OVP : 18.059V

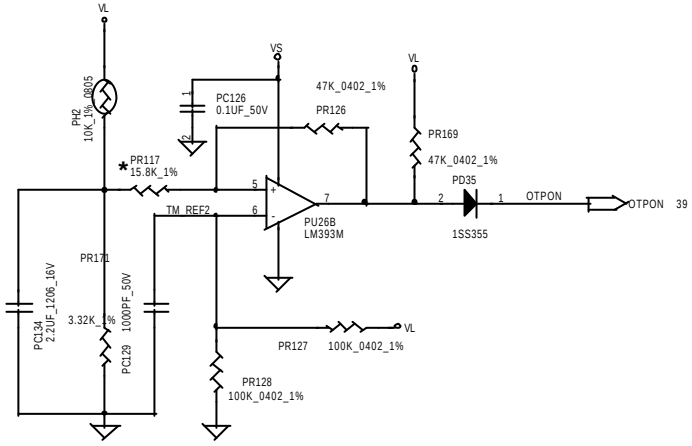




PH1 under CPU botten side :
CPU thermal protection at 76 degree C
Recovery at 45 degree C

PH2 near main Battery CONN :
BAT. thermal protection at 82 degree C
Recovery at 45 degree C





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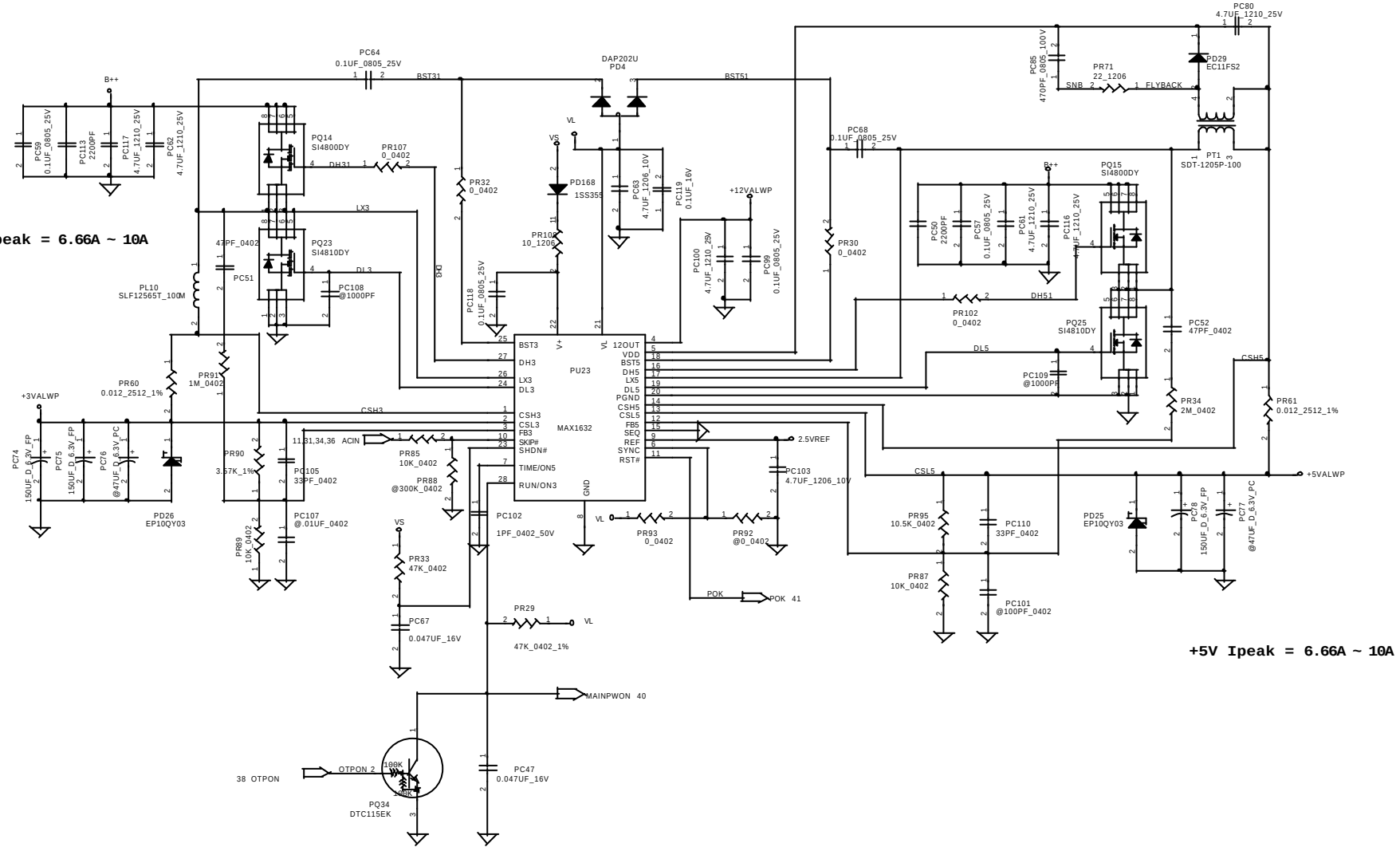
+3.3V/+5V/+12V



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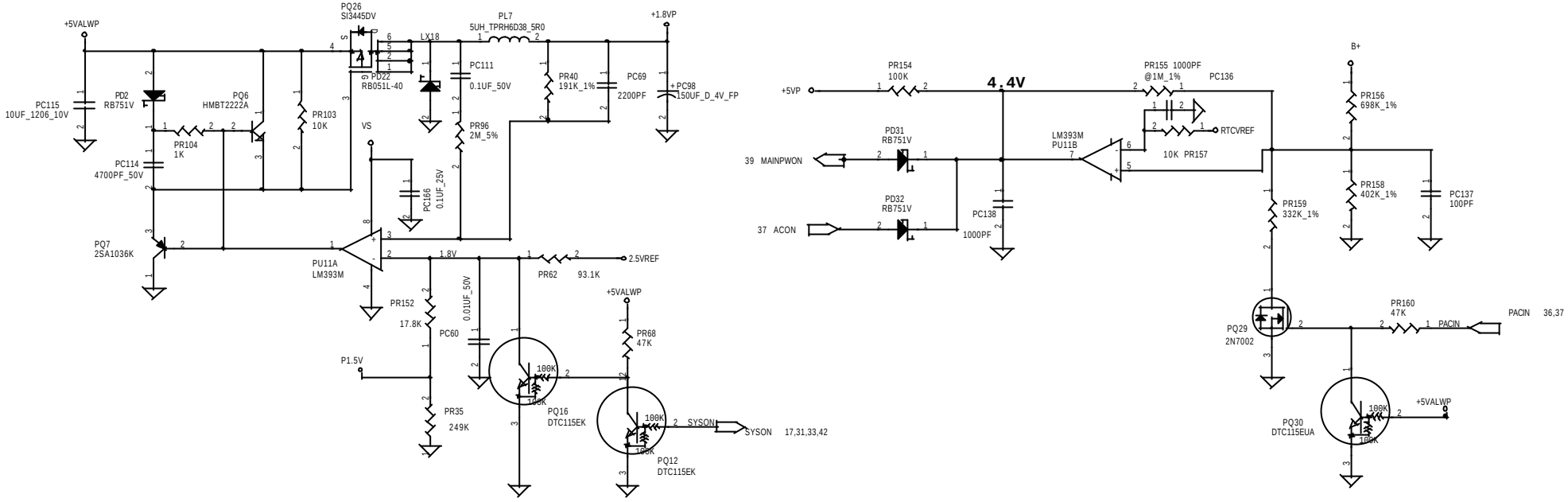
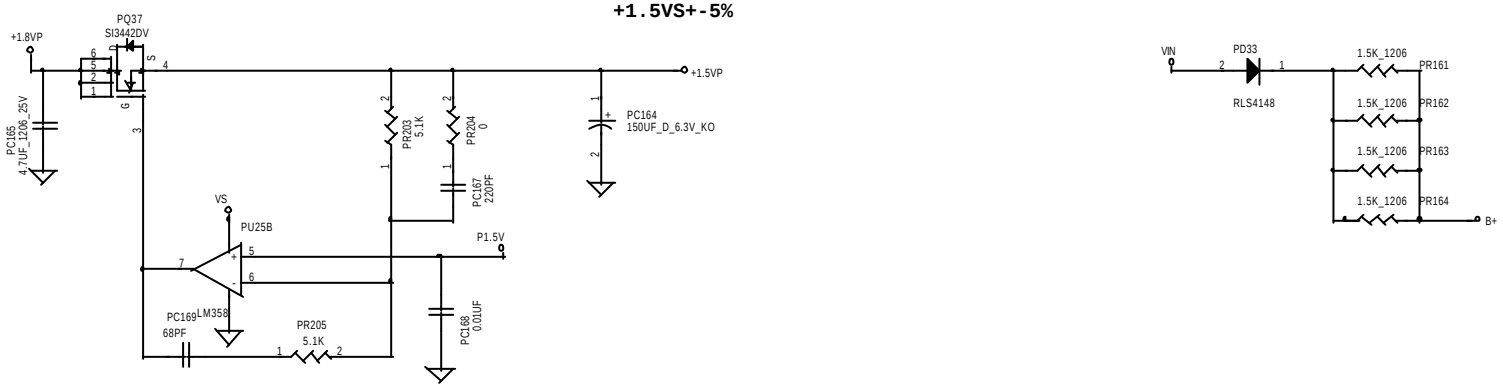
1.8V/1.5V

+1.8VP+-5%



+1.5VS+-5%



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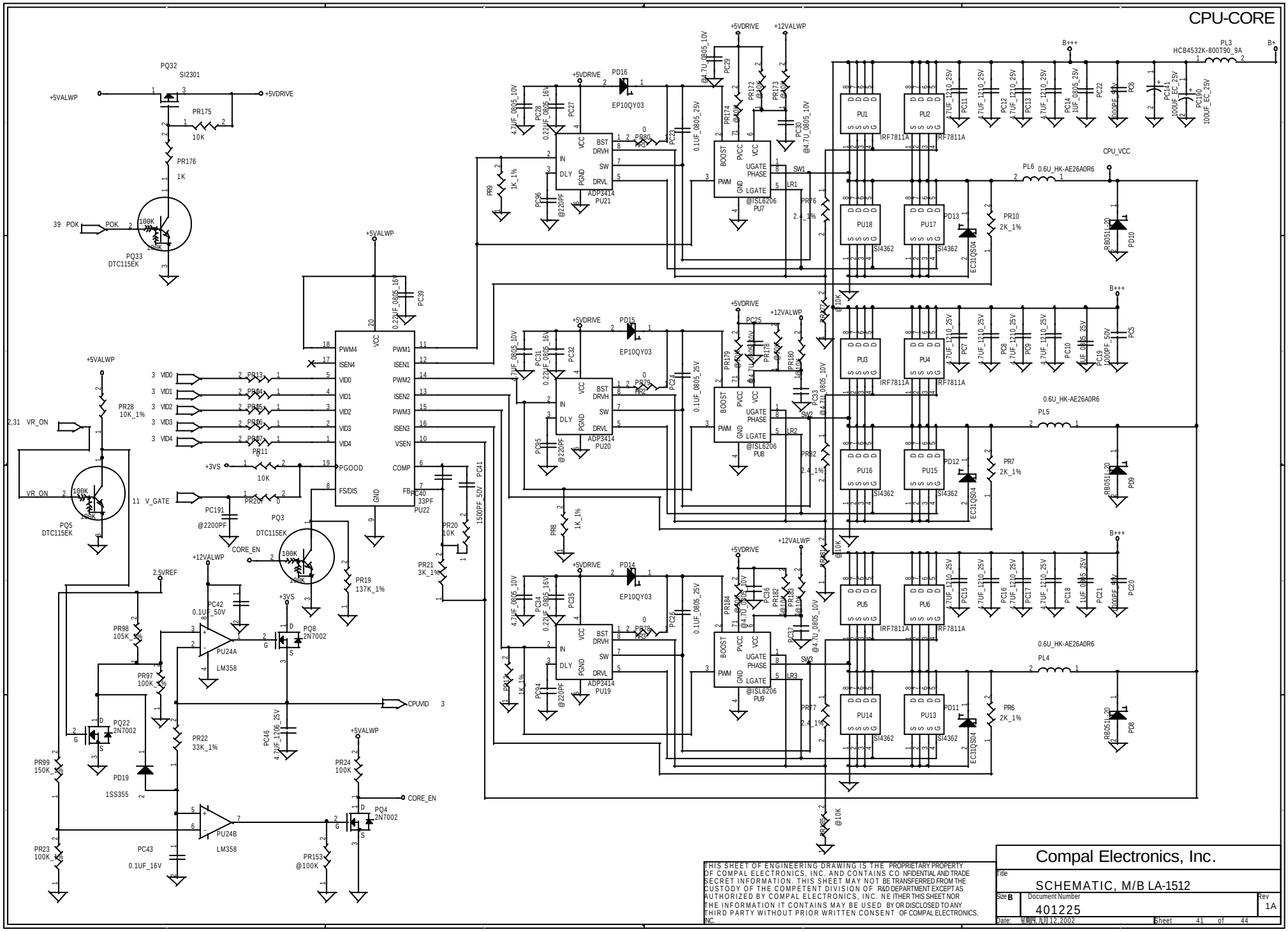

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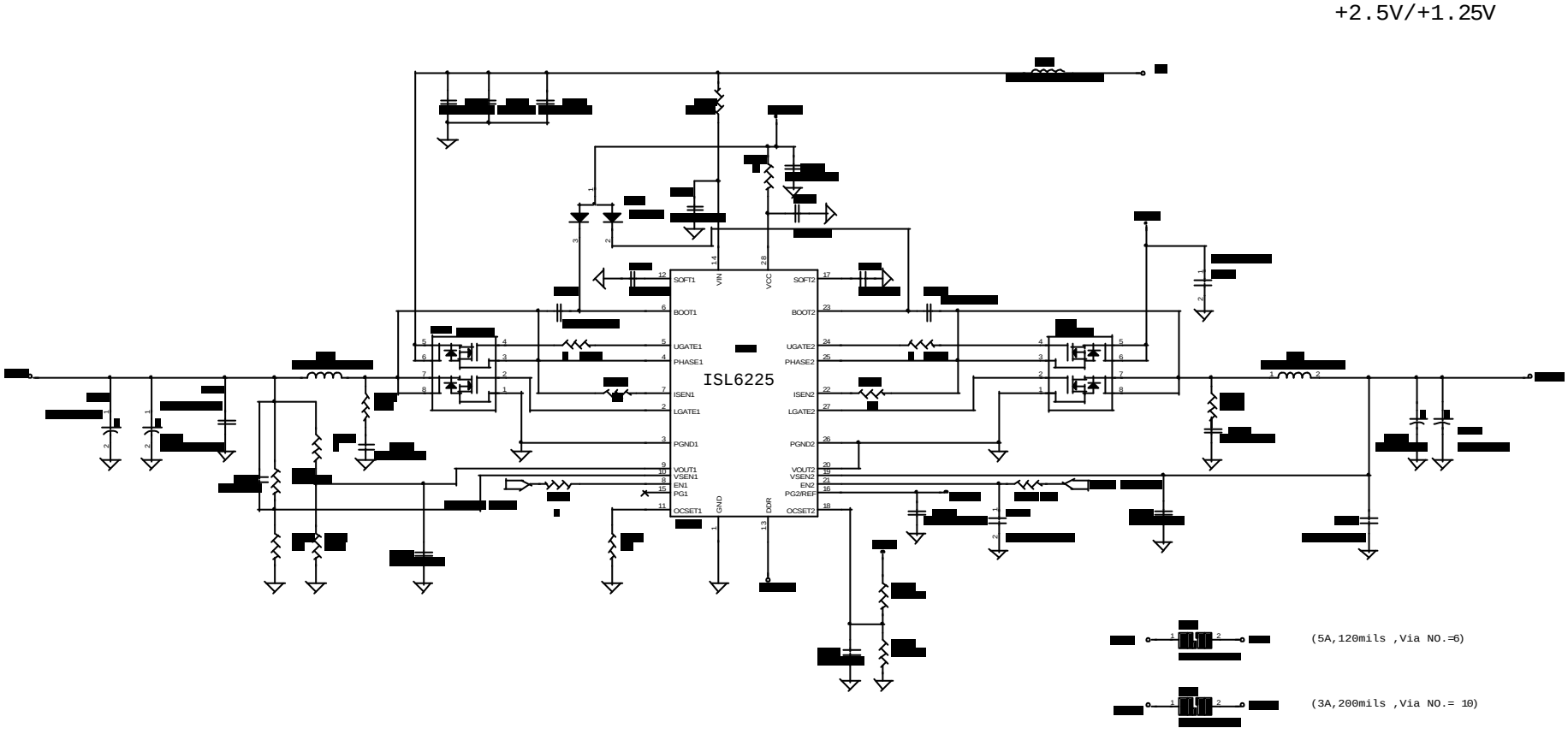

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ATR11 PIR LIST

HW PIR LIST

ATEST 9/6~

1	+2.5V LEVEL ERROR	Remove R111 100ohm Change R108 from 100 to 0 ohm	P15
2	SDRAM BANK select error	Change CLK_SDRAM3 from U22.F3 to U22.E3 Change CLK_SDRAM5 from U22.H5 to U22.G5 Change RRAS#3 from U22.H7 to U22.F7 Change RRAS#5 from U22.G6 to U22.H6	P5
3	Add CPU VCCVID pin	Add R492 connect to U23.AF3	P3
4	TV OUT output error	Change CRMA from U8.AF15 to U8.AF16 Change LUMA from U8.AF16 to U8.AF15	P12
5	Add MK1707 output terminate	Add R494 22 ohm	P12
6	Add low pass filter for MK1707 power pin	Add L47	P12
7	Change VGA option resistor to jumper	Change R284 to J3 Change R286 to J4 Change R295 to J5 Change R296 to J6	P15
8	Reserve +2.5V option control	Add R495 for SYSON control Add R496 for SUSP control	P15
9	Change LCD connector type	Change JP1	P16
10	Add TI TPS2042 for USB protect cicuit	Add U56(TPS2042)	P25

BTEST

PWR PIR LIST

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1		Creat +5VP power		36	Add PC192: 0.1UF; PZD5: RLZ5.1B PR208: 10K; PR209: 150K		DVT
2		Meet spec. of ISL6225 DDR2.5V Vsense voltage 0.89V		42	Change PR195 from 17.8K to 18.2K		DVT
3		For CP mode		37	Change PR64 from 10K to 4.7K PC121 from 4700PF to 1000PF		DVT
4		For DDR 1.25V ripple voltage		42	Change PC153, PC154 from 150uF/6.3V to 220uF/2V		DVT
5		For DDR 2.5V voltage		42	Add PC156: 220uF/2V; delete PC155: 220uF/2V		DVT
6		For cost downe		42 40	Change PL15 from 1.5uH SPC_06703 to 1.5UH TPRH6D38 Change PL7 from 5uH SPC_06703 to5UH TPRH6D38		DVT
7		For DDR 1.25V voltage sense		42	Change PR191 from 6.8K_1% to 2K_1%		DVT
8		For transient response of DDR 2.5V 1.25V		42	Add PC195 PC194 4.7uF/6.3V; de-pop PC153 Change PC193 from 1000pF to 4700pF; PR186 from 10 to 51Ohm		PVT
9		For reduce CP mode noise		37	Change PC121 from 4700PF to 1000PF		PVT
10		Increase voltage margin on CTL of MB1887		37	.De-pop PR100		PVT
11		Change 1.8V to 1.85V P1.5V to 1.73V requested from H/W		40	Change PR62 from 100K to 93.1K PR152 from 43K to 17.8K PR35 from 215K to 249K		PVT

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